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On current-voltage and capacitance-voltage characteristics of metal-semiconductor contacts

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Abstract: It is expected the fact that the current following across metal-semiconductor (MS) rectifying contact named as Schottky barrier diode (SBDs) and effect of sample temperature on their electrical properties obey thermionic emission (TE) current model. But, it has been seen that the abnormal behaviors in the measured electrical characteristics cannot be exactly understood by the classical TE transport theory. In the literature, the observed abnormal behaviors have been successfully explained by a Gaussian distribution function and by the pinch-off model being interaction of the neighbor patches suggested by Tung and coworkers, the named discrete regions model as “patches” with low barrier placed in a higher uniform barrier area.

Key words: Metal-semiconductor contacts, Schottky contacts, Schottky barrier diodes, rectifying contact, Schottky barrier height, barrier inhomogeneity, characteristics diode parameters

1. Introduction

A metal/semiconductor (MS) contact has the rectifying or ohmic nature. Schottky barrier diode (SBD) is called the rectifying MS contact and it is a device based on majority carriers. The forward biased Schottky contact (SC) allows the current to flow in one direction after a specific voltage but it is rectified the current in the opposite direction in reverse bias case. Accordingly, the SBDs are ideal for rectifier power electronic circuits. The fact that it is based on the majority of carriers provides a great advantage in terms of speed. However, the SBDs are widely used in radio frequency and other power electronics applications. In the case of forward biased, the SBDs have much higher current density than the pn junction diodes under the same potential difference [1–7]. In addition, they have an important place in the opto-electronics industry due to their ease of manufacture and general knowledge of the electronic properties. That is, the MS contacts form the basis of optoelectronic circuit structures such as MOS (metal-oxide layer-semiconductor) or MIS (I: insulating layer) capacitor or structures, FETs (field effect transistors), MESFETs (metal-semiconductor FETs), MOSFETs, solar cells, photodiodes, MFIS (metal-ferroelectric-insulator-semiconductor) structures, MFISFET memories, pn junctions, heterojunctions [8–14].

In 1874, *Braun* discovered and firstly described rectifying behavior of MS contacts. The MS contacts were used as radio detectors until the 1900s and then as radar detectors, and it was 1970s that they began to be used as microwave diodes. Schottky revealed, in 1938, with the Schottky barrier (SB) model that the potential barrier in the MS contact is caused only by stable space charges in the semiconductor rather than a chemical layer. Bethe developed the rectification theory of carriers for thermionic emission (TE) over this

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energy barrier in 1942 [1,6,8]. Later, Crowell and Sze [8] combined the current theories of Schottky and Bethe in a single TE-diffusion model. In order for a device to be used in technology, it is very important to know its characteristics parameters. The current transport mechanism across MS contact depends on the ideality of the fabricated MS junction, and it is determined from the electrical measurements with sample temperature. To fully understand the electrical properties and behavior of a SBD, the experimental electrical measurements must be taken at different sample temperatures and the characteristic diode parameters must be evaluated from these measurements [15–21].

It is well known that a SBD must be specially fabricated to be an intimate MS contact, but a thin native oxide layer forms at MS interface during fabrication of the MS contact, this interfacial layer has a strong effect on the diode characteristics and thereby the MS contact studies such as MIS diode [2,22,23]. Bardeen has explained how a SC independent of the metal work function Φ_M could form due to the effect of the trap states on semiconductor surface and at the MS interface [8]. He also showed that the contact potential can be a linear function of the Φ_M if there are the absence of surface states or sufficiently low surface state density. Goodman [24] has inspected the effect of a bias-independent surface state charge on the BH measurement from the variation of the barrier capacitance with the applied voltage. Crowell and Sze [25] showed how the bias dependence of the BH that results from the interface states and MS interface affects the diode $C-V$ relationship. The interface state density distribution (ISDD) has been firstly determined by Crowell and Roberts [9] using the $C-V$ characteristics of Au-Si diodes without regarding their $I-V$ characteristics.

Levine [26] has mentioned that the abnormal $I-V$ data are consistent with a barrier model in which there is an exponential ISDD, using the $I-V$ data of Au/ n -GaAs SBD reported by Padovani [27], did not consider consistency of his result with the $C-V$ characteristics of the analyzed diode. Borrego et al. [5,28] suggested a model for calculating the ISDD from the bias-dependent current and capacitance data of the guarded Au/ n -GaAs devices together with the deep traps in the potential barrier layer, and the interface states are in interaction with the metal. Horvath [4] has applied the analysis of Card and Rhoderick [2] to the reverse branch $I-V$ data and calculated the ISDD from the reverse and forward data of the MS contacts by making special suggestions on the ISDD.

Moreover, Meade et al. [22] supposed a new theory from the nonideal $I-V$ data of the MS contacts caused by the bias dependent interface state population and the MS SC potential barrier. Tseng and Wu [29] examined the effects of an interfacial layer and the interface states on the MS rectifying contact characteristics and discussed the bias dependent interface state population and determined the ISSD in the semiconductor band gap from the nonideal $I-V$ characteristics. Chattopadhyay and Daw [11] have inspected the $I-V$ data of MIS diodes with a native oxide layer including pinhole at MS interface and for the determination of its thickness. Then, the characteristics of Cd-doped Mg-Zn₃-P₂ SBDs have been interpreted [30] using the method in Refs. [11,29] and considering an interfacial layer with the interface states in action with the semiconductor substrate.

Eglash et al. [31] have mentioned the importance of the barrier height (BH) modification in engineered SBDs. They have reported that the reduced barrier diodes also allow as small signal zero-bias SBDs and microwave mixers, and that in one microwave SBD applications, that the traditional diodes having larger BHs must be used with a dc offset voltage, and furthermore, that the raised barrier structures can be used in the gates of MESFETs, and will result in raised noise margins, and that the small SBH normally causes very large gate leakage currents [15,32–35]. Moreover, as mentioned above, the raised barrier devices and diodes are also useful in surface recombination studies and may also be useful as optical detectors such as solar cells and photodiodes.

Furthermore, the high-BH SBDs and bipolar $p-n$ junctions can be used in determination of minority-carrier lifetimes and carrier diffusion constants.

It is stated that the $C-V$ data of an ideal SC is the applied frequency independent and increases with increment of the forward bias. However, this ideality is often deteriorated due to a interfacial layer and interface states at MS interface and the lateral inhomogeneity of BH [29,36–38], and the diode series resistance [11,39–41]. On the other hand, the series resistance R_s of the semiconductor bulk also plays an important role on behavior of the experimental $C-V$ and $I-V$ data of the SBDs [38,41,42]. Some authors have reported the formation of a peak in the forward $C-V$ curves. Ho et al. [38] has ascribed the origin of such a peak to the interface states, and Chattopadhyay et al. [11,42] and Chattopadhyay [37] to the series resistance effect and interface states.

Norde [43] has introduced a method for determination of the R_s from the forward branch $I-V$ curves with a ideality factor of $n = 1$. There are the disadvantages of this method because it considers only ideal diodes ($n = 1$), and the minimum of the function $F(V)$ cannot exactly be determined [44–47]. Sato and Yasumura [44] taken into account the Norde's function $F(V)$ that n can be greater than unity [43]. Their analysis [44] requires two $I-V$ curves at two different temperatures and determination of the minima in the modified Norde function. Still, the problem of the certain extraction of the minimum of the $F(V)$ function is existing [41,48–50]. Cibils and Buitregio [51] introduced another approach with another ancillary function $F(V) = (V - V_a \ln I)$ to the value of n and R_s . This model was still subject to the accuracy of fixing the minimum from the graph of $F(V)$ versus V plot. Then, adaptation methods given in Refs. [45] and [46] still has disadvantages of the determination of the minimums of the function curves as indicated in Ref. [52].

Paoli and Barnes [39] and Cheung et al. [40] suggested a different method and extracted the diode parameters from curves which are linear functions of the TE current expression. The plots [39,40] are calculated from the high voltage forward $I-V$ curve data which results from the MS interface properties and series resistance [11]. It has been purposed [41] the possibility of direct prediction of the series resistance from the current and conductance data. Although each models mentioned above has its own advantage according to other models, they have common limitations in the prediction of minimum points of the graphical and in their inappropriate methods, and/or they expose to a limitation that cannot be carried out a MIS or MOS [41,48–50]. The inconvenience and uncertainties associated with the graphical method suggest that the model developed by Chattopadhyay et al. [42] is a suitable one for determination of the R_s from the forward $I-V$ characteristics and high frequency forward $C-V$ curves of nonideal MS contacts.

Ayyıldız et al. [47] has considered the applied voltage drop across the insulating layer as well as the depletion region to calculate an exact value of the R_s , extending the analysis of Cheung method [40]. The diode parameters obtained in this way have been compared with those obtained without considering the MS interface properties. Then, Kiuru et al. [53] has suggested another new model for the thermal resistance and series resistance of a SBD. Durmuş and Atav [54] have suggested a method for determining the bias dependent behavior of the series resistance of a SBD from the $I-V$ data by help of TE equations. They [54] have made definition of the relative merit of the method by applying the method on some artificial $I-V$ data sets corresponding to known R_s values and comparing their own conclusions with the other methods. Recently, Oruç and Altındal [50] have applied Norde [43], Bohlin [45], Mikhelashvili [55], and Cheung [40] methods to $I-V$ data to determine the main parameters of a SBD. They [50] have concluded that the determined parameters generally depend on the used model. They have indicated from the obtained results that directly used standard

$I - V$ method is especially limited by the R_s value.

It is well-known that some diode parameters of SBDs are calculated by the TE current expression. Therefore, some studies have also intensified on the nonideal $I - V$ characteristics [17,21,56–73]. There are many studies on the diode parameters as a function of the sample temperature [18,65,74–82]. The SBDs with low BH have found applications in MS contacts studying at cryogenic temperatures as infrared detectors and sensors in thermal imaging [17,70,74,83–85]. Thereby, the use of the $I - V$ data at only one temperature does not give intended information about transport mechanism across device, and the nature of its potential barrier formation. The measurements in the sample temperature environment allow us to understand a number of aspects of transport mechanism across device as well as electrical properties of the device. However, a detailed definition of the conduction mechanism of a diode is still a difficult problem. The investigation of the $I - V$ data of a MS diode by means of the conventional TE current generally reveals an abnormal reduction in the BH Φ_b and an increment in the ideality factor n towards low temperatures [15,34,86–95] which causes nonlinearity in the arrhenius activation energy plot $\ln(I_0/T^2)$ vs. $(kT)^{-1}$. The reasons of the undesirable nonidealities in $I - V - T$ measurements [67,96–104] have been successfully investigated by means of the modified TE current with Gaussian distribution (GD) of the BHs.

Song et al. [105] has firstly explained the abnormal behaviors depending on the measurement parameters at the MS contacts by a GD model of spatially inhomogeneous BHs. These measurement parameters are temperature and bias voltage. It has been mentioned that the potential barrier change can occur by the inhomogeneity of the interfacial oxide thickness and its composition and interfacial charge distributions [105]. They [105] have obtained the effective Richardson constant (RC) values considering temperature coefficient of BH and using the modified TE expression by the GD function. It has been introduced a new analytical model related to potential fluctuations for the explication of $I - V$ and $C - V$ data of the PtSi/Si SBDs by Werner and Guttler [57]. They [57] have used the differences of $C - V$ and $I - V$ BHs at each temperature by a value of the standard deviation of the GD. Tung et al. [64,106] and Tung [64,65] have regarded a system of “patches” with low barrier height as well as higher uniform barrier across SC. Sullivan et al. [107,108] have indicated that the interaction between neighboring patches should causes pinch-off of the current transport path of small low BH regions embedded in high barrier. In such cases, the reverse or forward bias current through a low-BH patch regions arises by the change of the height of the “saddle point” emerging by the interaction between patches rather than the local BH at the MS interface [20,60,65]. The “pinch-off” is a terminology often stated to define the working of a FET. That is, Tung [20,60] has given the comprehensive review and in-depth discussion on the formation, structure and concept of the SB from both physics and chemistry viewpoint. Finally, Gorji and Cheong [109] have considered and discussed a review of theoretical and fabrication progress on the last two decades for contact production with placed nanoparticles (NPs) to investigate the NPs effects on the transport mechanism and electrical properties of SCs.

It has been mentioned in Refs. [57,60,65,70,93,99,100,105] that the spatially inhomogeneous of BH is likely to be a function of the interface atomic structure and inhomogeneities at the SC interface caused by nonuniformity of the interfacial charges, grain boundaries, multiple phases, facets, defects, a mixture of different phases etc. The existence of small local regions (“patches”) with different BH has been shown by using ballistic electron emission spectroscopy (BEES) [110]. Furthermore, Talin et al. [111] have also determined the nanometer-resolved lateral changes in the barrier height by the BEE microscopy and have compared the spatial profile and the statistical distribution of the BHs of Au/ n -GaAs SD to the macroscopic barrier height from the

current-voltage and capacitance-voltage curves of the same SC.

However, Werner and Guttler [57] and Sullivan et al. [107,108] and Tung [60] have not presented any information by their own approaches related to how to extract RC value of the semiconductor substrate used in a SC fabrication. Chand and Kumar [70] have discussed the temperature-dependent current-voltage curves of Pd_2Si SC on both n - and p -type Si by the modified TE-diffusion current mechanism by the GD of BHs, following Refs. [105] and [57]. They [70] directly used a plot of the apparent BH versus $(kT)^{-1}$ to calculate the zero-bias standard deviation and the mean BH using the current barrier heights without regarding the capacitance-voltage data, and they have modified the classical Richardson equation under the prediction of GD of BHs.

Moreover, Iucolano et al. [112] and Roccaforte et al. [113] have inspected the $I-V-T$ curves of Pt/GaN and $\text{Ni}_2\text{Si}/4\text{H-SiC}$ SBDs, respectively, and have discussed that the prediction of the RC value can be related to the formation of a lateral inhomogeneous SB caused an effective area lower than the total area of the SC for the current flow across the device, and they [112,113] have determined the expected value of the RC value from the modulated Richardson plot using the different value of A_{eff} at each temperature by help of Tung's model. Kumar et al. [114] have determined the value of the RC value in the InN nanodot-Si heterojunction by Tung's model by following Roccaforte et al. [113]. Recently, for Mo/ p -GaTe SCs, Gülnahar and Efeoglu [115] have obtained the RC value from the modified Richardson plot by Werner and Guttler's approach [57] using the temperature-dependent standard deviation values. Soyulu and Yakuphanoglu [116] have studied a statistical study on the barrier heights and ideality factors of the room temperature forward bias current-voltage curves of Au/ n -GaAs SC. They have showed that the current equation for inhomogeneous SCs in terms of the model of Sullivan et al. [108] and Tung [64,65] models displays an exact fit to this $I-V$ characteristics. Korucu et al. [90] have presented the $I-V$ curves of an Au/ n -GaAs SCs in 80–320 K range, and have interpreted the temperature-dependent $I-V$ curves of the diode by help of the modified TE method, accounting for the possible existence of a nanometer-sized “patches” distribution following Refs. [108] and [60,65]. Recently, Kavasoglu et al. [117] have evaluated the variations of SBH by using GD, and have obtained total current by performing numerical integration taking contributions from each elementary diode. They have studied the random multidiode model for Au/ n -GaN device, and have assumed the device to have spatially inhomogeneous barrier height, and have considered that the changes in barrier heights of elementary diodes distribute as random, and have argued that this kind of distribution can be a more realistic approximation to real Schottky contact because it is probable that random distribution of BHs of elementary diodes becomes around the mean value within the distribution limits.

The model of potential fluctuations for inhomogeneous SCs [57,105,108] differs from earlier models suggested by Odomari and Tu [118] who have inspected the parallel connections of discrete and homogeneous SCs with different values of the BH. They [118] have stated that the total DC current across the patch-like arrangement of low-barrier NiSi/Si and high-barrier PtSi/Si SCs can be modeled by adding the low-barrier current, and the high barrier current. Furthermore, Im et al. [92] have also determined both the expected macroscopic diode $I-V$ characteristics and nm-scale BH distributions (BHDs) resulted from specific “patch parameter” distributions, following the Tung model. Their studies [92] have mentioned that both the microscopic and macroscopic behaviors for relatively ideal SCs can be defined by the Tung model with a large coverage ($>5\%$) of shallow patches, the determined BHDs are nearly similar for relatively ideal and highly nonideal SCs, and a simple Tung model can elucidate highly nonideal behavior only by prediction of an unphysical patch distribution

in which the excess current is satisfied by a few patches in the extreme tail of the patch distribution. Horváth [119] stated by numerical simulation that the lateral GD of BHs by model given in Ref. [57] can be explained by the domination current with an anomalous high level of TFE via the junction with the same accuracy. He also suggested a method for the determination of diode parameters such as BH, effective RC, characteristic emission energy, and bias-dependent BH from the $I - V$ curves by help of the TFE [20,60,77,94,102,120,121].

Donoval et al. [122] have measured the current-voltage curves of PtSi-Si SC in 90–350 K range, and have stated that the contributions of TE current and the other current conduction expressions such as the generation-recombination, tunneling and leak currents caused by inhomogeneities and defects at the MS interface must be considered in evaluating the SBH. Thus, they have achieved an outstanding agreement between theory and experiment, and more exact values of the TE saturation current and thus the SBH in a wide temperature range.

The purpose of this review paper can be stated as follows: As mentioned above, the current following across MS rectifying contact named as SBD usually obeys TE current model. The characteristics diode parameters such as BH, ideality factor, series resistance and RC and their temperature-dependent are generally determined and interpreted by means of TE current theory. It has been well-known that the determined values of the parameters of the real diodes usually deviate from expected values. Therefore, we have focused on the literature which successfully explain the abnormal behaviors of the $I - V$ characteristics using an analytical potential fluctuation model with GD based on spatially inhomogeneous BHs [70,105,123], and which consider the pinch-off model named as interaction of some neighboring small “patches” with the low barrier embedded in the higher uniform barrier area [65,107,108].

2. Theoretical background

A rectifier MS contact is often referred as Schottky barrier diode (SBD), or shortly Schottky contact (SC). Let us consider a metal/ n -type semiconductor rectifying contact. When a metal with a work function $q\Phi_m$ comes in contact with a semiconductor with a work function, $q\Phi_s$, a charge transfer occurs until the Fermi levels (FLs) reach the same level. For example, when the $q\Phi_m > q\Phi_s$, the FL of the semiconductor is higher than that of the metal before contact, that is, the FL of the semiconductor is then above the FM of the metal by an amount $(q\Phi_m - q\Phi_s)$. After contact, a charge exchange occurs; the electrons from the semiconductor surface layer enter the metal, leaving ionized donors behind in that surface layer. As can be seen from Figure 1a, a depletion region width (w) forms in the n -type semiconductor near the junction region. The positive charge due to unbalanced donor ions within the depletion region matches the negative charge on the metal surface. The bending of the bands due to the electric field in the depletion region has features similar to those of $p - n$ junction.

The energy difference between Φ_m and $q\Phi_s$ confronts electrons as a potential difference that must be overcome after thermal equilibrium is achieved, this $q(\Phi_m - \Phi_s)$ is also called qV_0 equilibrium contact energy on the semiconductor side. This diffusion potential barrier V_0 prevents further net electron diffusion from the semiconductor conduction band (CB) to the metal. The potential BH that the electrons need to exceed in order for the electrons to pass from the metal to the semiconductor side is $q\Phi_b$ and is equal to the difference $q(\Phi_m - \chi_s)$, where $q\chi_s$ called electron affinity is measured from the vacuum level to the semiconductor CB minimum. The diffusion potential V_0 can be reduced or raised by applying forward or reverse voltage, as in $p - n$ junction.

Metal/ n -type semiconductor/metal (M/ n/n^+) contact is a structure with the $p - n$ diode properties, such a structure is called shortly the MS Schottky diode. The M/ n/n^+ structure is formed by making metal

rectifier contact on one surface of n -type semiconductor material and electron-rich nn^+ ohmic back contact on the other surface. Energy-band diagram of such a structure in thermal equilibrium is seen in Figure 1. When a voltage such as $V < 0$ is applied to the n^+ ohmic-back contact side, the structure is forwardly biased. Similarly, when a voltage such as $V > 0$ is applied to the n^+ ohmic-back contact side, the structure is in reverse bias state. As seen in Figure 2, the potential BH for electrons is equal to $q\Phi_b = e(V_d + E_f)$, where V_d is diffusion potential and $E_f = V_n$ is the potential difference between the FL and minimum of the CB in the neutral region for an n -type semiconductor.

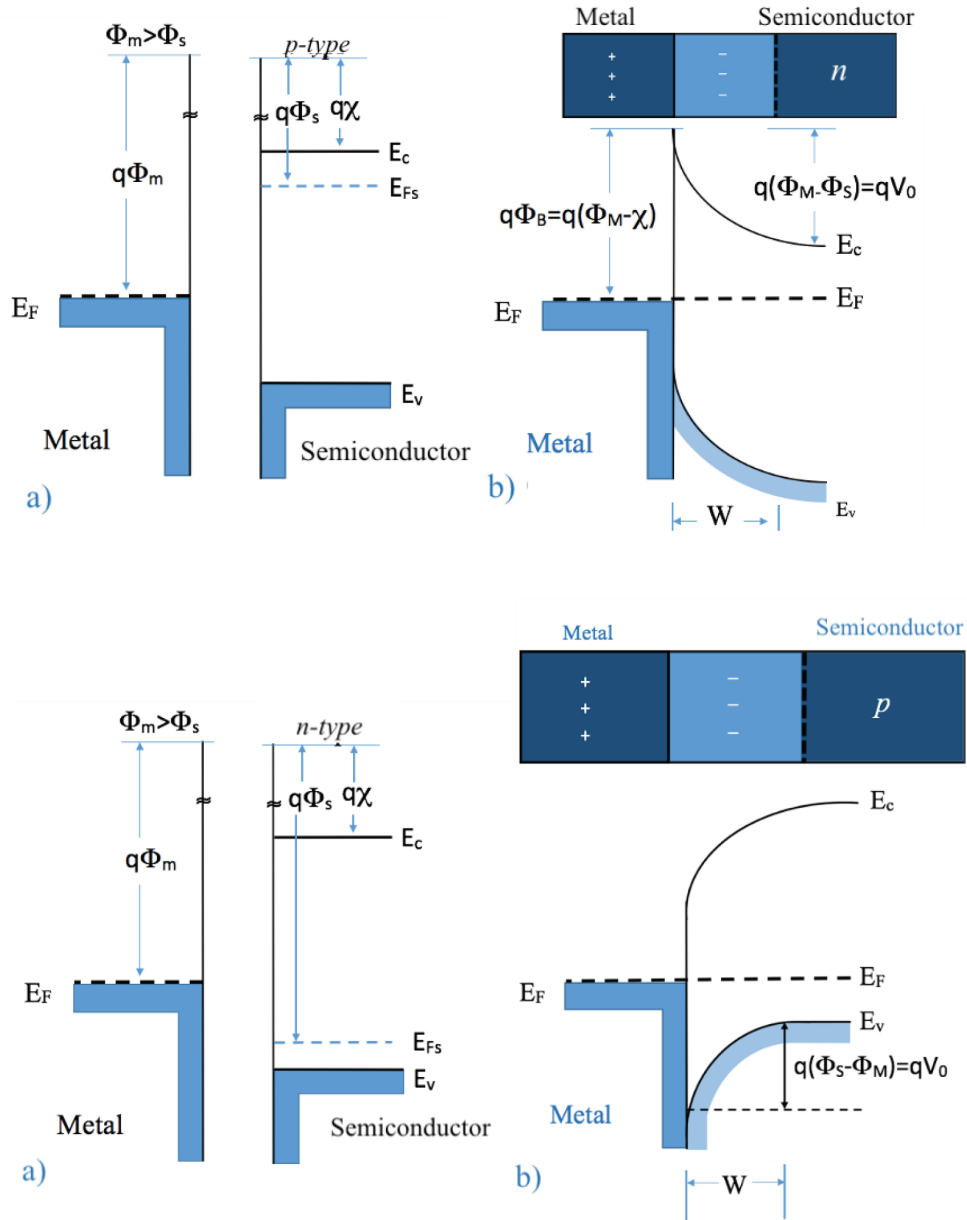


Figure 1. The energy band diagram of a metal/ n -type semiconductor and a metal/ p -type semiconductor, a) before contact, b) in after contact.

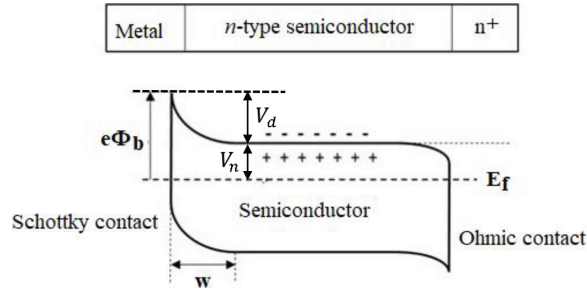


Figure 2. Energy-band diagram of metal/*n*-type semiconductor/metal structure in thermal equilibrium.

2.1. Comparison of Schottky barrier diodes and *p*-*n* junction diodes

The choice between Schottky barrier diodes (SBDs) and *p* – *n* junctions is generally determined by the technological aspects for opto-electron device applications, sometimes both have to be technologically viable and then the choice between them must be made according to the electrical properties. Let us compare a SBD and a *p* – *n* junction. These have the same barrier height, and have been made from a moderately doped *n*-type semiconductor. We suppose that the *p* side of the *p* – *n* junction has more lightly doped than the *n* side. As well known, the current in a *p* – *n* junction is determined by the diffusion of minority carriers while the current in a SBD by TE of majority carriers over the barrier height. That is, in a metal/*n* type SBD, the current is carried almost entirely by majority carrier electrons. In practice, the BH of a *n*-Si based SBD is in the range 0.5–0.6 eV, while that of a *p* – *n* junction made from the same Si is about 0.8 eV. Thus, the saturation current I_0 of a SBD for the same BH exceeds that of a silicon *p* – *n* junction by a factor of about 10^3 . For the same current value, the forward voltage drops across the *p* – *n* junction exceeds by at least 0.4 V that across the SBD diode. This makes the SBD particularly suitable for use as a high-current and low-voltage rectifier device; and the *p* – *n* junction as a high-voltage and low-current rectifier device. Thereby, since the reverse saturation current is also larger for the SBD, a SBD is not as suitable as a *p* – *n* junction for use a high-voltage and low-current rectifier [124,125].

2.2. Current-voltage equations in SBDs

The considered conduction mechanisms for analyzing the current flow across a SBD are thermionic emission (TE), thermionic field emission (TFE) and field emission (FE). The TE current occurs by thermal activation of charge carriers over the potential barrier; the FE current is based on the quantum mechanical effect and the charge carriers directly tunnel through the potential barrier under an electric field influence. The current in the TEF occurs by a combination of both TE and FE regimes. The charge carriers in TEF mechanism are thermally activated to a region thin enough for efficient tunneling through the potential barrier [57,65,70,108,109].

Let us consider the metal/*n*-type semiconductor/metal (MS) structure in Figure 2. At first, in thermal equilibrium case, some electrons with the thermal energy which have enough thermal energy to cross the potential barrier give rise to equal and opposite currents I_0 , from the metal side (SC) into the semiconductor and from the semiconductor side into the metal SC. In nonequilibrium case, that is, under a bias voltage, the electron current from the SC metal side into the semiconductor is independent of bias, that is, the current must not exceed the saturation current, I_0 . However, the electron current from the semiconductor side into the metal SC depends strongly upon bias.

In the forward bias, the ohmic-back contact side is negatively biased, the potential barrier in the semiconductor side falls by eV for the electrons crossing from the semiconductor into the metal, and now the potential barrier is $e(V_d - V)$, where V_d is the diffusion potential. Thus, while the electron current from the SC metal side into the semiconductor is $-I_0$, for zero bias, the electron current from the semiconductor side into the SC metal is $+I_0 \exp(eV/kT)$. The net current in the forward bias case comes up as [1,84,124,126]

$$I = I_0 \left[\exp\left(\frac{e(V - IR_s)}{nkT}\right) - 1 \right]. \quad (1)$$

In reverse bias case, that is, the ohmic-back contact side is positively biased, the potential barrier in the semiconductor side arises by eV , and the net reverse bias current comes up as

$$I = I_0 \left[1 - \exp\left(-\frac{e(V - IR_s)}{nkT}\right) \right], \quad (2)$$

where I_0 is the saturation current and is given by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right), \quad (3)$$

where $q\Phi_b = e(V_d + V_n)$ are the effective barrier height (BH) at zero bias and n ideality factor. Eqs. (1) and (2) are called the TE current ones, where k is the Boltzmann constant, T is the absolute temperature, the $q\Phi_b$ and n are calculated from the intercept and slope of the linear portion of the semilog forward bias $\ln I - V$ curves, respectively, A^* is the effective RC. For example, A^* is $32 \text{ Acm}^{-2} \text{ K}^{-2}$ for the p -Si and $8.16 \text{ Acm}^{-2} \text{ K}^{-2}$ for n -type GaAs; A is the diode area. R_s is the series resistance of the neutral region of the semiconductor substrate in a SC. The $(V - IR_s)$ and IR_s are the voltage drop across the depletion region and the R_s , respectively. The downward curvature region of the forward bias $I - V$ curves at high forward bias results in from the R_s , as can be seen from the $I - V$ curves in Figure 3.

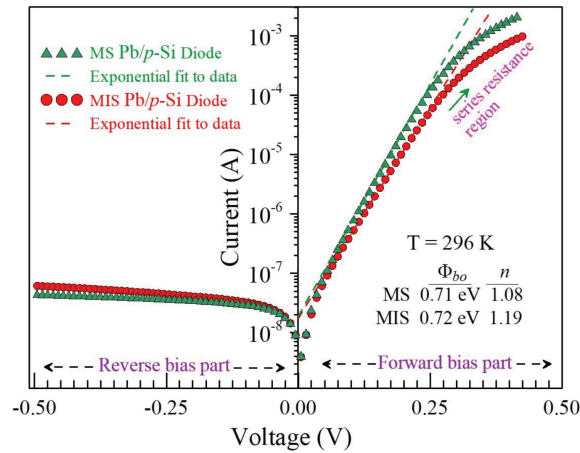


Figure 3. Forward and reverse bias $I - V$ plots of the MS and MIS Pb/ p -Si/Al Schottky contacts at 296 K. Average free carrier density of $N_A = 5.32 \times 10^{15} \text{ cm}^{-3}$ for the used p -Si wafer was determined from the $C - V$ measurements, and the corresponding resistivity value was $\rho_p = 2.62 \text{ } \Omega\text{-cm}$.

As well-known, if the surface of a semiconductor substrate used in the MS contact fabrication is prepared by the usual polishing and chemical etching, and the metal evaporation is carried out in a conventional vacuum

system having about 10^{-5} torr pressure, the semiconductor surface is inevitably covered with a thin native oxide film between 10 Å and 30 Å depending on the surface preparation method. The interfacial layers can be also formed by water or vapor adsorbed onto the semiconductor surface before insertion in the vacuum system [36,124,127]. The MS contacts fabricated under these conditions are not intimate contact because the oxide film inevitably separates them [81,128]. For a sufficiently thick interface layer, the interface states are in interaction with the semiconductor rather than the metal [2,129–131]. Figure 3 represents the $I - V$ plots of the MS (metal-semiconductor) and MIS (metal-insulating native oxide layer-semiconductor) Pb/*p*-Si/Al Schottky diodes at 296 K. For formation of the insulating native oxide layer in the MIS contact, the front-side of the *p*-Si was exposed to clean room air at room temperature for three days before Schottky contact fabrication.

The values of the barrier height from the semilog forward bias $I - V$ curves for the MS and MIS SBDs in Figure 3 were calculated as 0.71 and 0.72 eV, respectively, using Eq. (3). The n value of the MS and MIS diodes was calculated as 1.08 and 1.19 from the slope of the linear portion of the semilog forward bias $I - V$ curves in Figure 3, indicating that the R_s effect in this region was not important. The n value of 1.19 indicates that the device obeys a MIS diode type rather than an ideal SC. The value of 1.19 for n usually lead to films of thickness of the order of 20–30 Å [130,132].

Ideality factor n is a measure of compatibility of pure TE. The deviation of the n from unity may be due to different reason including TFE, recombination current effect, barrier inhomogeneities effect, image force lowering effect and the interfacial effects [60,68,95,133]. In the recombination case, such departures become more obvious at low temperatures and low forward-bias voltage. Moreover, at low temperature, in heavily doped semiconductor substrate, the forward bias current arises from the tunneling of electrons with energies above the bottom of the CB. If the temperature is raised further, the effect of tunneling is negligible, and the current across diode can be pure TE [60,126].

The ideality factor is an indicator of the bias dependence of the SBH. The bias-dependent of the effective SBH can be caused by the electric field in the depletion region even in a MS contact. The barrier height Φ_b becomes the bias-dependent in the presence of an interfacial layer and barrier inhomogeneity. Thus, most of electrons will flow directly into the metal for a TE current to form, while some of electrons are trapped by the interface states due to the interfacial layer. This event causes modification in the effective BH (decrease or increase), thereby increasing or decreasing the diode current [127,134–138]. In other words, the occupation of the interface states causes a change in the space charge density in the depletion region, inducing change of the potential across the interfacial layer, and thus the reverse current unsaturates, the forward and reverse branch $I - V$ curves become nonideal. We will return to this topic later in barrier inhomogeneity part. In such a case, the $I - V$ characteristics will modify. Thereby, we can write as $\Phi_b = \Phi_{b0} + \beta V$, the coefficient $\beta = \frac{\partial \Phi_b}{\partial V}$ is the voltage coefficient of Φ_b and always is positive because Φ_b arises with increment in forward bias; and declines with increment in reverse bias and thus the reverse current unsaturates. Thus, the current expression in Eq. (1) becomes

$$I = I_0 \exp\left(-\frac{\beta q V}{k T}\right) \left[\exp\left(\frac{q V}{k T}\right) - 1 \right] \quad (1)$$

$$I = I_0 \exp\left(\frac{q V}{n k T}\right) \left[1 - \exp\left(-\frac{q V}{k T}\right) \right], \quad (2)$$

where n is the ideality factor and is expressed by

$$\frac{1}{n} = (1 - \beta) = \left(1 - \frac{\partial \Phi_b}{\partial V}\right), \quad (3)$$

and I_0 saturation current represents the zero bias current from Schottky metal side to semiconductor substrate, at the forward biased Schottky contact case, and it is given by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right). \quad (4)$$

Thus, the reverse bias TE current equation is given by

$$I = I_0 \left[1 - \exp\left(\frac{-eV}{nkT}\right)\right]. \quad (5)$$

When the BH is bias-dependent, the effective BH Φ_e should be used in place of the Φ_{b0} in Eq. (4), and thus the voltage dependent expression of the BH, Φ_e is given as

$$\Phi_e = \Phi_{b0} + \left(1 - \frac{1}{n_1}\right)V, \quad (6)$$

where $\left(1 - \frac{1}{n_1}\right) = \frac{\partial \Phi_b}{\partial V}$. Eq. (6) generally affects at $eV > 3kT$ region in the reverse-biased Schottky contact, but the ideality factor n in Eq. (5) will be only effective at $eV < 3kT$ region in the reverse bias part, and at $eV > 3kT$ region in the forward bias part of the $I - V$ curves. The so-called ideality factor n_1 includes the contributions from other current transport mechanisms [4,127,131,139,140]. The multiplier $\left(\frac{V}{n}\right)$ in Eq. (2) or (5) is the voltage drop across diode; and only across the depletion region in the ideal diode case and then $n = 1$.

The theoretical $I - V$ curves of the reverse bias have been formed considering the voltage dependent change of the BH and the voltage drop across the depletion region using Eqs. (5) and (6). Figure 4 represents the theoretical semilog $I - V$ curves of the reverse bias formed using Eq. (5) for the bias independent SBH and a temperature of 296 K.

The ideality factor in Eq. (5) ranges from $n = 1.00$ to $n = 3.50$ with steps of $\Delta n = 0.50$. Figure 5 displays the theoretical semilog reverse bias $I - V$ curves at 296 K, where (a) and (b) theoretical curves have been drawn using Eq. (5), the SBH in the (a) and (b) curves is the bias independent with $n = 1$ and 3.5, respectively; and the curves (c) and (d) have been plotted with $n_1 = 1.032$ in (6) and $n = 1$ and $n = 3.50$ in Eq. (5); the barrier height in the (c) and (d) curves is the bias-dependent. Figure 6 demonstrates the experimental and theoretical semilog reverse $I - V$ curves at 296 K, for the MS and MIS diodes in Figure 3. The bias-independent theoretical curve for $n = 1$ in Figure 6 is plotted using Eq. (5), at 296 K. The theoretical fit curves to the experimental $I - V$ curves of the MS and MIS diodes in Figure 6 have been plotted using Eqs. (5) and (6); $n = 1.70$ and $n_1 = 1.0145$ for the fit to the experimental MS $I - V$ curve, and $n = 2.81$ and $n_1 = 1.020$ for the fit to the experimental MIS $I - V$ curve. The (c) and (d) curves are unsaturated due to the bias dependent-barrier height.

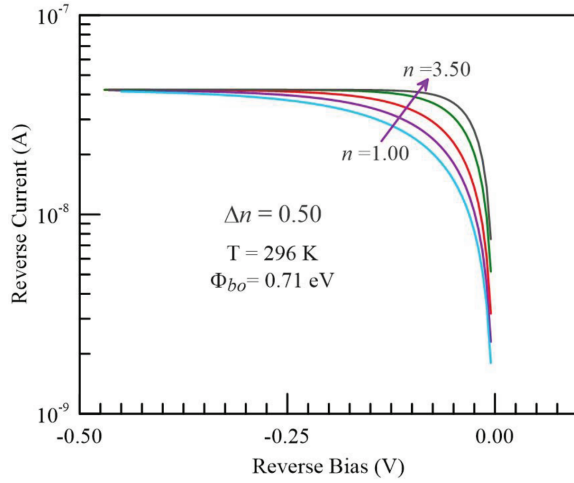


Figure 4. Theoretical $I - V$ curves of the reverse bias with Eq. (5) from $n = 1.00$ to $n = 3.50$, $\Delta n = 0.50$ at 296 K, where the barrier height is the bias-independent.

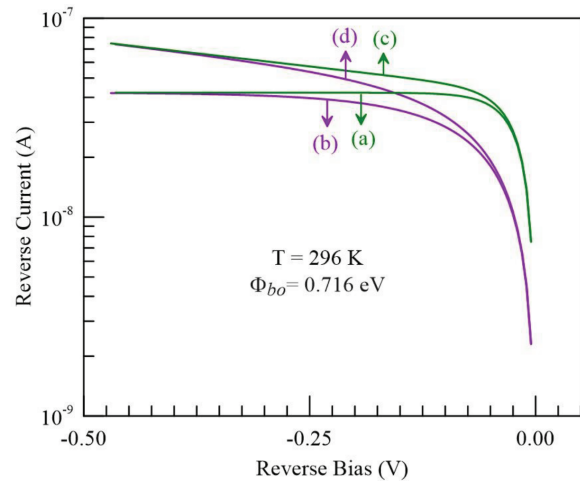


Figure 5. Theoretical $I - V$ curves reverse bias at 296 K. (a) and (b) theoretical plots were formed using Eq. (5), the barrier height for the (a) and (b) curves is the bias-independent with $n = 1$ and 3.5 , respectively. Curves (c) and (d): $n = 1$ and $n = 3.50$, respectively, with $n_1 = 1.032$ using Eqs. (5) and (6); the barrier height in the (c) and (d) curves is the bias-dependent, Eq. (6)

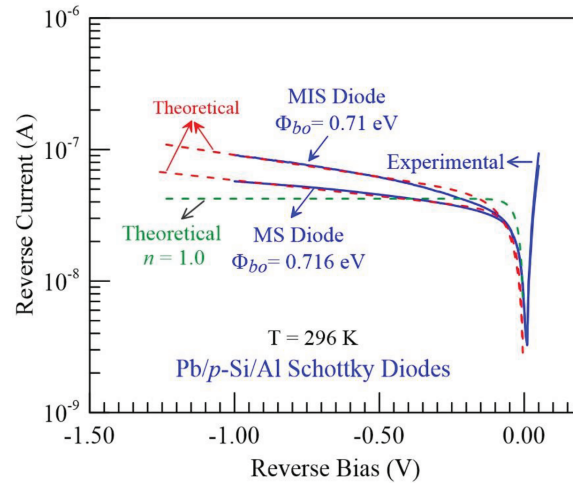


Figure 6. Theoretical and experimental $I - V$ curves of the reverse bias at 296 K, for the MS and MIS diodes. The bias-independent theoretical curve for $n = 1$ is plotted using Eq. (5), at 296 K. The theoretical fit curves to the experimental $I - V$ curves of the MS and MIS diodes were plotted using Eqs. (5) and (6); $n = 1.70$ and $n_1 = 1.0145$ for the MS diode, and $n = 2.81$ and $n_1 = 1.020$ for the MIS diode.

2.3. The dependence of current-voltage characteristics on measurement temperature

If the $I - V$ data of a SC can be explained by the conventional TE current equations, the SBH of such a diode is frequently laterally homogeneous, such a SBD behaves almost such as an ideal diode behavior at temperatures around 300 K, and it offers to determine the expected diode parameters and to test the validity of the Schottky barrier theories. The SBH and ideality factors have been found to vary with change of the measurement temperature. It is usually assumed that the temperature-dependence n can give the information about the current transport mechanism of a SBD [22,65,97-99,141-145]. As well known, the current transport across

the MS Schottky contact is an activation process of the carriers under temperature effect, the current carriers at low temperatures are able to surmount the lower barriers. Therefore, the current will predominantly flow through the lower barrier height and larger n at low temperatures. At higher temperatures, the BH will be a function of the bias voltage and temperature [20,137,146]. In such a case, the deviation of the expected ideal current behavior can be explained by assuming the presence of the spatially inhomogeneous BHs and potential fluctuations at the interface that consist of low and high barrier areas. That is, the temperature dependent changes may be considered by the concept of the lateral barrier inhomogeneities with TE theory [22,69,147–150]. It can be adopted two different approaches to describe spatially inhomogeneity of the SBHs. One of them assumes that a continuous spatial distribution of the apparent BH and the total current across the MS Schottky contact is simply calculated by integrating the current determined by the ideal TE model with an individual BH and weighted by the Gaussian distribution (GD) function [33,57,98,148,151–154]. Using the GD, the total current is described approximately by the modified TE theory with an apparent BH and n being a function of temperature. This approach can successfully explain usually anomalous behaviors observed in the $I - V$ characteristics, such as a reduce of SBH and an increment in ideality factor due to decrease in temperature, the difference of SBH determined from different methods, the nonlinear Richardson activation curve. The other approach by Tung [65] and Sullivan [98,107,108] dominates at small bias and especially low temperature; and assumes the presence of some small patches with the placed low SBH in the mean SBH area [72,73,103].

It has been reported that the experimental BHs Φ_{eff} and ideality factor values n obtained from the $I - V$ characteristics differ from diode to diode even if they are identically prepared on the same semiconductor substrate, and that this relationship between Φ_{eff} and ideality factors is an evidence to the presence of the spatially inhomogeneous of BHs and potential fluctuations at the MS contact interface that consist of low and high barrier areas. In such a case, it has been seen that the BHs of these diodes linearly decrease with increasing ideality factors. Mönch [155] and Schmitsdorf et al. [56] and some authors [83,95,156–158] have also theoretically and experimentally calculated the lateral homogeneous BH value of the diode from the linear relationship between the BHs and ideality factors of identically prepared diodes on the same semiconductor wafer. This finding was attributed to patchy of interfaces or to lateral inhomogeneities of the Φ_{eff} [65,136,159]. Tung [65] says that these results are hard to explain with interface gap states because these are usually assumed to have implications in the determination of the BH and ideality factor of a SBD diode. The linear relationship between the obtained Φ_{eff} and ideality factors is an evidence for the presence of the spatially inhomogeneous BHs and potential fluctuations at the MS contact interface.

Figure 7 shows Φ_{eff} versus ideality factor plots of the identically produced Pb/ p -Si Schottky contacts on the different pieces cut from the same semiconductor substrate, (a) for 67 dots from MS Schottky diodes, (b) for 33 dots of MIS Schottky diodes prepared on the p -Si piece with the native oxide layer. The forward and reverse bias current versus voltage curve of one of the MS and MIS Pb/ p -Si/Al Schottky diodes at 296 K have been given in Figure 3. An interesting case is that the data of the MS and MIS Pb/ p -Si/Al Schottky dots in Figures 7a and 7b fall on the same straight line, as can be seen in Figure 7c. The laterally homogeneous BH values of 0.74 and 0.72 and 0.75 eV for the MS and MIS and Pb/ p -type and MS plus MIS Schottky dots have been obtained from the linear relationship between experimental effective BHs and ideality factors in Figures 7a–7c.

In the next section, we will point to the experimental $I - V$ measurements of the nonannealed and thermally 400 °C annealed Co/ n -GaAs/In SBDs whose $I - V$ characteristics depend on measurement temperature in 60–320 K range. These $I - V - T$ characteristics will help us to understand the ideal TE current model and

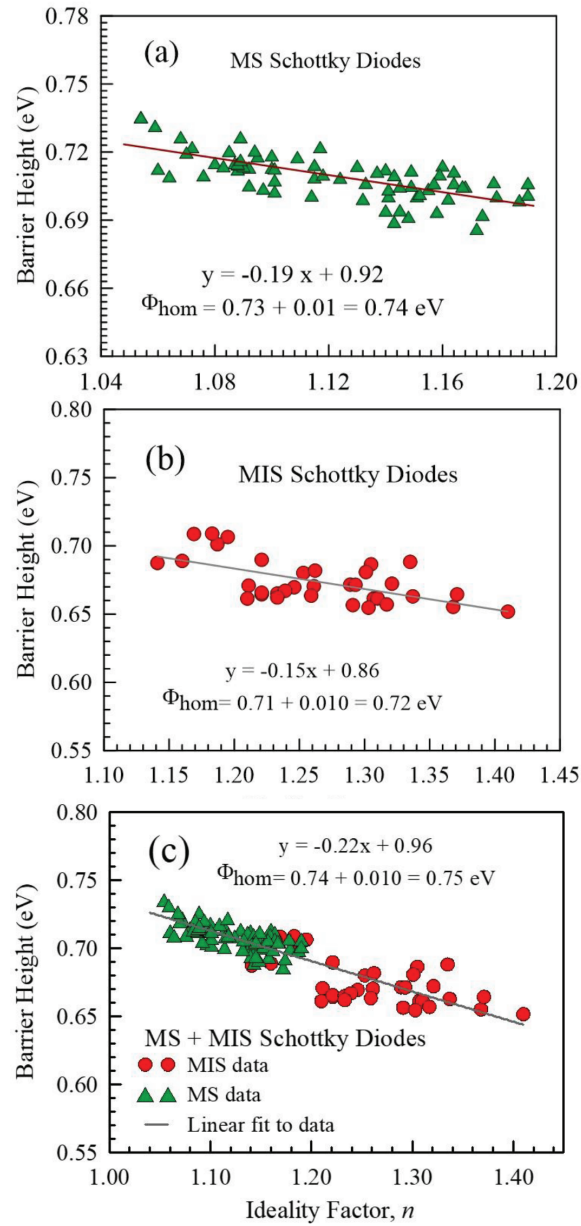


Figure 7. Φ_{eff} versus ideality factor plots of identically produced Pb/ p -Si Schottky contacts on the same p -type Si substrate.

spatially inhomogeneous BHs model based on ideal TE current and Cheung and Cheung's [36] and Norde's [43] series resistance models. We have indicated that these deviations can be explained by the models based on the presence of the spatially inhomogeneous BHs and potential fluctuations at the interface that consist of low and high barrier areas [160–165].

Let us now consider the temperature-dependent $I - V$ characteristics of the Co/ n -GaAs/In SBD given in Figure 8. The $I - V$ measurements were made from 60 K to 320 K at 20 K intervals. The experimental details are given in Ref. [146]. The SBH and ideality factor and series resistance values at some temperatures for this SBD are tabulated in Figure 8. The SBH and ideality factor versus temperature plots of this diode are given

in Figure 9. As can be seen, the ideality factor is very close to unity from 320 K to 140 K, and the SBH value approximately remains unchanged from 100 K up to 320 K. This suggests that the current flow dominantly obeys the TE in this temperature range [146,156,166]. But, at temperatures from 100 K down to 60 K, the barrier height value decreased while the ideal factor value increased.

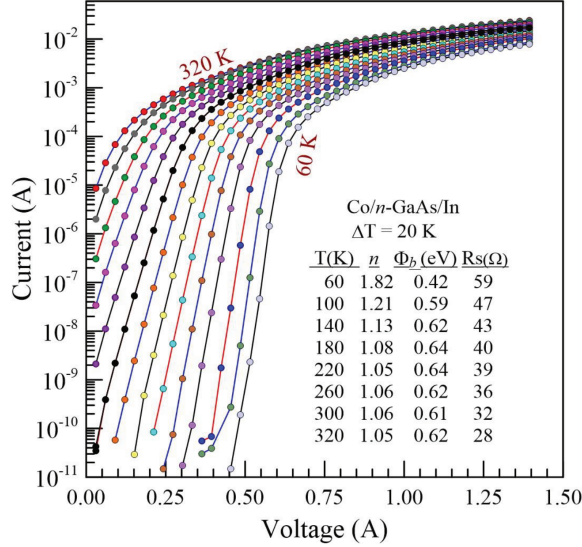


Figure 8. $I - V$ curves of the forward biased Co/ n -GaAs/In SBD from 60 K to 320 K at 20 K intervals.

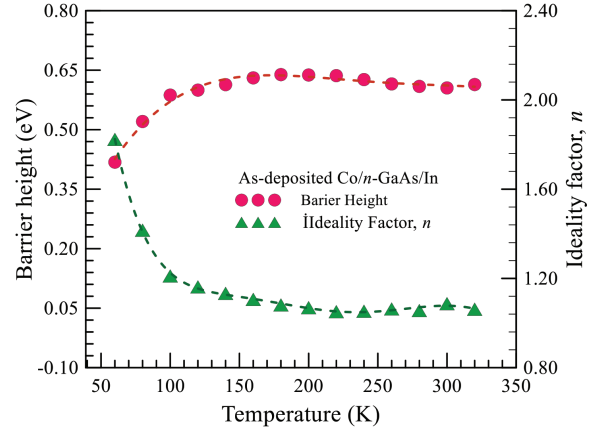


Figure 9. Apparent barrier height and ideality factor as a function of measurement temperature from the $I - V$ measurements in Figure 7.

It may be assumed that the contact interface consists of small local regions with BH of 0.42 eV at 60 K and 0.52 eV at 80 K and 0.59 eV at 100 K through which charge carriers prefer lower local regions due to the lateral inhomogeneity of the barrier heights with a decrease in temperature. It has been suggested that the current flow through these small regions may be accepted as a tunneling type current at lower temperatures [88,89,167–169]. Therefore, we can say that the current with increasing temperature dominantly flows by the TE over the main barrier, and the current through these small regions is more important at temperatures below approximately 120 K for this diode [103,150,170,171]. Horvath et al. have said that the fact that the apparent BH and n depend remarkably on the temperature at low temperatures can be related either to the lateral barrier inhomogeneity or to the dominantly TFE [119,166,172].

The Co/ n -GaAs/In SBD was thermally annealed at 400 °C. The temperature-dependent $I - V$ characteristics of the 400 °C annealed Co/ n -GaAs/In SBD are given in Figure 10. The $I - V$ measurements were made from 60 K to 320 K at 20 K intervals. The characteristic diode parameters are tabulated in Figure 10. As mentioned above, it is seen from Figure 11 that the SBH reduces linearly with temperature. This shows the presence of an interfacial thin layer formed at metal/ n -GaAs interface due to the thermal annealing [40,84,173,174]. For example, these are the values of $n = 1.06$, $\hat{\Phi}_{b0} = 0.61$ eV and $R_s = 32 \Omega$ of for the as-deposited Co/ n -GaAs diode, and the values of $n = 2.53$, $\hat{\Phi}_{b0} = 0.80$ eV and $R_s = 133 \Omega$ for the annealed diode, at measurement temperature of 300 K.

It has been said in literature that the usual temperature dependence of the SBH in n -type SBDs is the same as that of the band gap, i.e. the BH increases with increasing temperature [14,123,148,175,176]. It is seen from Figure 11 that the SBH value for the annealed diode linearly reduces with decreasing temperature while it

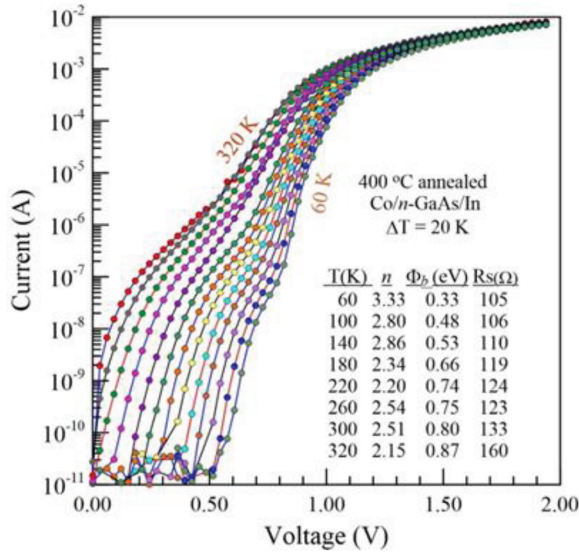


Figure 10. Forward biased $I - V$ characteristics a function of measurement temperature of the 400 °C annealed Co/ n -GaAs/In SBD.

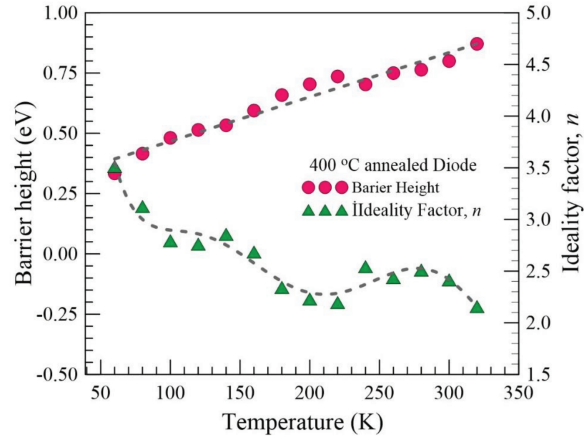


Figure 11. Apparent barrier height and ideality factor as a function of the measurement temperature from the $I - V$ characteristics of 400 °C annealed SBD in Figure 9.

approximately remains unchanged from 100 K to 320 K. Therefore, we can say that formation of the SBH and its change with the measurement temperature also depend on the interface properties of the MS contact. Horvath et al. [119,172,177] have indicated that the increment in the electric field at the semiconductor surface may be geometrical inhomogeneities as crystal defects, surface roughness or the device periphery (edge effect), a local pile up of dopant atoms (e.g., around crystal defects), a doping concentration increment in the near-interface region, the formation of an inversion layer at the interface, a transitional (alloyed or heteroepitaxial) surface layer with other parameters than the bulk semiconductor, the presence of a relatively thick insulator interfacial layer with low dielectric constant, and the fixed interface charge one and interface state charges. The interface statedensity may also be affected by a transitional surface layer and the MS interface quality. However, the lateral inhomogeneity of BH and/or the local increment of electric field result in a lower effective junction area [119,177].

Furthermore, Cheung and Cheung [40] have found and obtained the values of $n = 1.13$ and 1.40 , and the values of $R_s = 18.8 \Omega$ and 145.6Ω for the room temperature $I - V$ characteristics of the as-deposited W/GaAs and 700 °C annealed W/GaAs Schottky diodes, respectively. They [40] attributed the increment in n and R_s values to the diffusion of W atoms into the GaAs substrate to a depth of about 500 Å after 700 °C annealing, leading to the formation of a highly resistive layer at the W/GaAs interface, from Rutherford backscattering spectrometry (RBS) analysis. Thereby, we can be say that a highly resistive layer at Co/GaAs interface forms due to the 400 °C annealing.

Figures 12 and 13 represent the Richardson or Arrhenius $\ln(I_0/T^2)$ versus $(kT)^{-1}$ or $(nkT)^{-1}$ plots drawn by means of Eq. (7) of the as-deposited and annealed Co/ n -GaAs/In SBDs. The Richardson activation relationship is given by

$$\ln \left(\frac{I_0}{T^2} \right) = \ln(AA^*) - \frac{q\Phi_{bo}}{kT}. \quad (7)$$

The $\ln(I_0/T^2)$ versus $(kT)^{-1}$ plot should yield a straight line whose slope gives an effective BH and intercept the Richardson constant A^* , known value of $8.16 \text{ A}/(\text{cm}^2\text{K}^2)$ for n -type GaAs. Owing to the bowing of the curve below 120 K in Figure 12, the value of $\Phi_{eff} = 0.635 \text{ eV}$ was determined from the slope of the linear fit to the experimental data above 120 K. This value is in close agreement with average value of 0.62 eV of the BH values at temperatures above 120 K, which are values given in Figure 8.

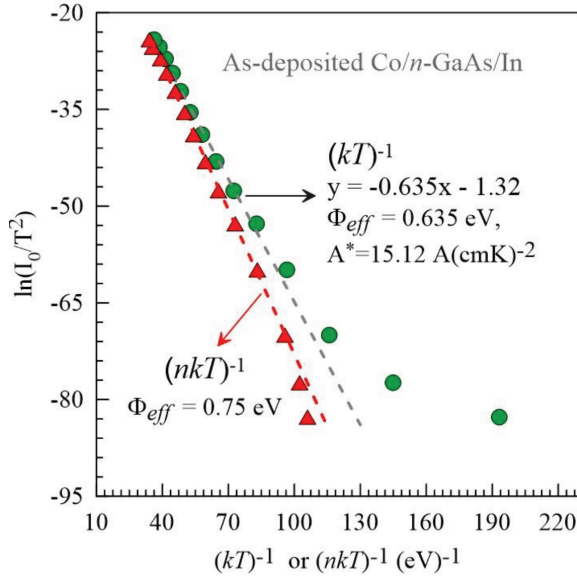


Figure 12. Richardson or Arrhenius plots; $\ln(I_0/T^2)$ versus $(kT)^{-1}$ or $(nkT)^{-1}$ curves of the as-deposited Co/ n -GaAs/In SBD.

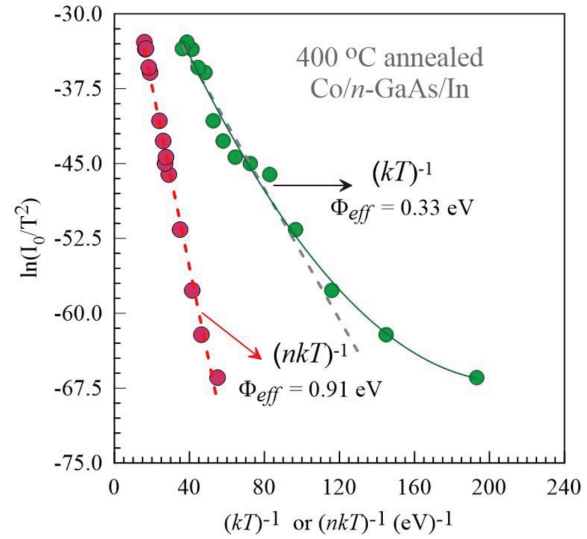


Figure 13. Richardson or Arrhenius plots; $\ln(I_0/T^2)$ versus $(kT)^{-1}$ or $(nkT)^{-1}$ curves of 400°C annealed Co/ n -GaAs/In SBD.

The value of $\Phi_{eff} = 0.75 \text{ eV}$ was determined from the slope of the straight line of the modified Richardson plot $\ln(I_0/T^2)$ versus $(nkT)^{-1}$ plot for the as-deposited diode. The intercept of the straight line part of $\ln(I_0/T^2)$ versus $(kT)^{-1}$ plot has given a Richardson constant value of $15.12 \text{ A}/(\text{cm}^2\text{K}^2)$, this value is approximately two times larger than the known value of $8.16 \text{ A}/(\text{cm}^2\text{K}^2)$ for n -type GaAs. $\Phi_{eff} = 0.635 \text{ eV}$ and $15.12 \text{ A}/(\text{cm}^2\text{K}^2)$ values from this plot are the expected values within experimental errors because the $I - V$ characteristics above 120 K of the as-deposited Co/ n -GaAs diode obey to the TE transport mechanism. That is, the current across the junction flows dominantly by the TE over the Schottky barrier.

The $\ln(I_0/T^2)$ versus $(kT)^{-1}$ plot for the 400°C annealed diode in Figure 13, has given a value of $\Phi_{eff} = 0.33 \text{ eV}$ determined from the slope of the fitted straight line to linear part of the data. The value of $\Phi_{eff} = 0.33 \text{ eV}$ is far from the values at high temperature values given in Figures 10 and 11. The value of $\Phi_{eff} = 0.91 \text{ eV}$ for the annealed diode was calculated from the slope of the straight line of the modified Richardson plot $\ln(I_0/T^2)$ versus $(nkT)^{-1}$ plot.

The bowing of the experimental $\ln(I_0/T^2)$ versus $(kT)^{-1}$ curve is reason of the temperature dependence of the BH and n . We will discuss in the following sections. The deviation in the Richardson plots may be due to the interfacial layer and interface states between MS rectifying contact interface [105,178]; and the spatially inhomogeneous BHs and potential fluctuations at the MS interface that consist of low and high barrier areas, that is, the current through the diode will flow preferentially through the lower barriers in the potential

distribution, when it is concerned the spatially inhomogeneity of BHs. As explained by Horváth [119,172,179], A^* value obtained from the temperature dependence of the $I-V$ characteristics may be affected by the lateral inhomogeneity of the barrier, and the fact that it is different from the theoretical value may be connected to a value of the real effective mass that is different from the calculated one. Therefore, these undesirable findings clearly indicate the deviation from pure TE current mechanism and hence further investigations are required to understand the observed behavior [15,61,71–73,77,96,153,180–182].

2.3.1. The inhomogeneous barrier analysis and mean barrier height in $I-V-T$ characteristics

The abnormal behaviors given above can be interpreted by the analytical potential fluctuation model with GD based on spatially inhomogeneous BHs at the MS contact interface [57,70,105,147,183]. The GD expression of BHs with a mean value of $\bar{\Phi}_{bo}$ and standard deviation σ_s has the form

$$P(\Phi_b) = \frac{1}{\sigma\sqrt{2\pi}} \exp \left[- \left(\frac{(\Phi_b - \bar{\Phi}_b)^2}{2\sigma^2} \right) \right], \quad (11)$$

The total forward bias current across the SC is then given by

$$I(V) = \int_{-\infty}^{+\infty} I(\Phi_b, V) P(\Phi_b) d\Phi_b, \quad (12)$$

where $I(\Phi_b, V)$ is the current for a given barrier Φ_b and bias voltage V . Substituting Eqs. (4) and (12) in Eq. (6) and performing the integration, the current relationship can be written

$$I(V) = I_0 \exp \left(\frac{qV}{n_{ap}kT} \right) \left[1 - \exp \left(- \frac{qV}{kT} \right) \right], \quad (8)$$

where

$$I_0 = AA^*T^2 \exp \left(- \frac{q\Phi_{ap}}{kT} \right), \quad (9)$$

and Φ_{ap} and n_{ap} are the apparent BH and ideality factor, respectively, and are given by

$$\Phi_{ap} = \bar{\Phi}_{bo} - \frac{q\sigma_o^2}{2kT} \quad (10)$$

$$\left(\frac{1}{n_{ap}} - 1 \right) = \rho_2 - \frac{q\rho_3}{2kT}. \quad (11)$$

It is stated that the mean SBH $\bar{\Phi}_{bo}$ and σ_s are linearly bias dependent on Gaussian parameters, such as $\bar{\Phi}_b = \bar{\Phi}_{bo} + \rho_2 V$ and standard deviation $\sigma_s = \sigma_{so} + \rho_3 V$, where ρ_2 and ρ_3 are voltage coefficients which may depend on T and quantify the voltage deformation of the BH distribution. The standard deviation is a measure of the barrier homogeneity and the lower value of σ_s corresponds to more homogeneous BH, and the temperature dependence of σ_s is usually small and can be neglected [71,87,100,101,156,184].

Figure 14 was plotted using the apparent BH data of the 400 °C annealed Co/ n -GaAs SBD in Figure 11. Thus, the plot of Φ_{ap} vs. $(2kT)^{-1}$ (Figure 14) according to Eq. (10) has given two straight lines with $\bar{\Phi}_{bo}$

and σ_o from the intercept and slope, respectively. One of them is at high temperature region (HT) in 140–320 K range and the other is low temperature (LT) region in 60–140 K range. The values of 1.04 eV and 110 mV for $\bar{\Phi}_{bo}$ and σ_o (the zero-bias standard deviation), respectively, were determined from the HT region in Figure 14. The value of $\bar{\Phi}_{bo} = 1.04$ eV is in close agreement with the value of 0.91 eV from the modified $\ln(I_0/T^2)$ versus $(nkT)^{-1}$ plot in Figure 13. Furthermore, the values of 0.69 eV and 61 mV for $\bar{\Phi}_{bo}$ and σ_o , respectively, were determined from the LT region in Figure 14. The lower value of σ_o corresponds to more homogeneous BH. Clearly, the diode with the best SC performance presents the best homogeneous barrier with the standard deviation with the lower value. It was seen that the value of $\sigma_o = 110$ mV is not small compared to the mean value of $\bar{\Phi}_{bo} = 1.04$ eV in the HT region, or the value of $\sigma_o = 61$ mV is not small compared to the $\bar{\Phi}_{bo} = 0.69$ eV in the LT region and this case indicates the presence of an inhomogeneous interface. On the other hand, the potential fluctuation and inhomogeneity generally have an effect on low temperature $I - V$ characteristics. The $\sigma_o/\bar{\Phi}_{bo}$ ratio is 0.106 in HT region while this ratio is 0.088 in LT region. It has been said that the barrier inhomogeneity in the annealed diode arises with increasing measurement temperature. The similar examples with two or more regions for the plot of Φ_{ap} vs. $(2kT)^{-1}$ have been also reported by other authors [70,185–187].

The existence of two GD regions in the SBDs was already experimentally proven by BEEM [188,189]. Vanalme et al. [190] have observed these changes at the chemically treated GaAs surface. Likewise, Chand and Kumar have accepted that each of such double and more GDs in the MS contacts has its own homogeneity nature [187,191]. This may involve variation in the MS interface composition/phase, interface quality, electrical charges and nonstoichiometry, etc. Furthermore, such inhomogeneities might occur on a scale that obstructs their detection by the usual characterization instruments. They are important enough to electrically influence the temperature-dependent $I - V$ and $C - V$ data of the SBD. Thus, the measurements at very low temperatures can reveal the nature of the barrier homogeneities found in the contact area. That is, the presence of a second GD at very low temperatures is probably due to some phase change occurring on cooling below a certain temperature. In addition, the temperature range covered by each straight line recommends the regime in which the corresponding distribution is effective. It has been reported in Refs. [60,192–194] that the variation of the diode parameters by thermal annealing may be attributed to changes of surface morphology and variation of nonstoichiometric defects at the interface vicinity and the formation of interfacial phases at the interface, and to the interfacial products that are formed at the interface.

Furthermore, the suitable values of the diode parameters such as the SBH and RC can be determined modifying the temperature dependent experimental values with the GD model. The nonlinearity in the conventional Richardson $\ln(I_0/T^2)$ versus $(kT)^{-1}$ plot at low temperatures can be resolved using Eq. (10) (the apparent BH Φ_{ap}) in Eq.(9) according to the GD of the BH. Thus, Eqn.(9) can be given as

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_o^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\bar{\Phi}_{bo}}{kT}. \quad (12)$$

The modified $\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_o^2}{2k^2T^2}\right)$ vs. $(kT)^{-1}$ plot for the 400 °C annealed Co/*n*-GaAs diode according to Eq. (12) is given in Figure 15 which consist of two regions as the HT and LT ones. The slope and intercept ($=\ln AA^*$) of this plot with two straight lines directly give the mean $\bar{\Phi}_{bo}$ and the RC value for a given diode area *A*. These values were determined as $\bar{\Phi}_{bo} = 0.69$ eV and $A^* = 9.35$ A/cm²K² for the LT region and $\bar{\Phi}_{bo} = 1.04$ eV and $A^* = 7.41$ A/cm²K² for the HT region. These values are in close consistency with the values of $\bar{\Phi}_{bo} = 0.69$ eV and $\bar{\Phi}_{bo} = 1.04$ eV obtained from the Φ_{ap} vs. $(2kT)^{-1}$ plot (Figure 14). The obtained values of

$A^* = 7.41 \text{ A/cm}^2\text{K}^2$ and $A^* = 9.35 \text{ A/cm}^2\text{K}^2$ for both regions are in close consistency with the known value of $A^* = 8.16 \text{ A/cm}^2\text{K}^2$ for the n type GaAs.

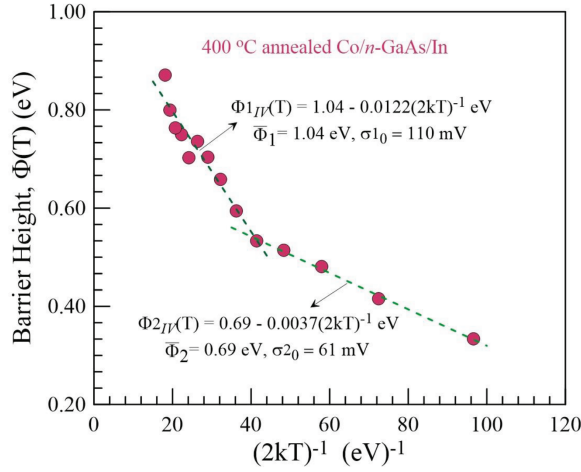


Figure 14. Plot of Φ_{ap} vs $(2kT)^{-1}$ according to Eq. (10) of the experimental apparent BH for the 400 °C annealed Co/ n -GaAs SBD.

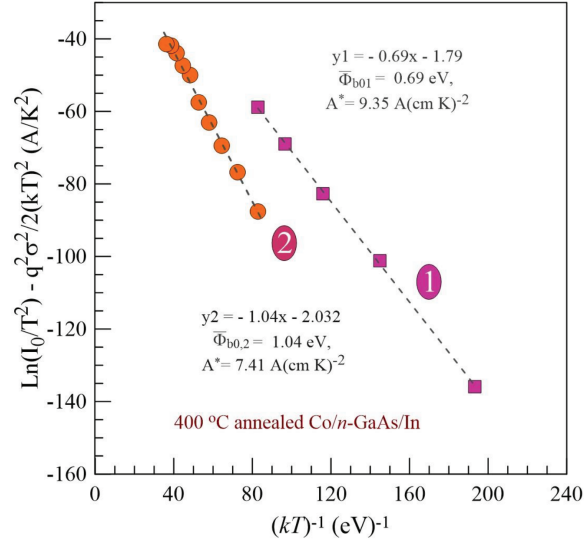


Figure 15. Richardson $\ln(I_0/T^2) - q^2\sigma_s^2/2k^2T^2$ versus $(kT)^{-1}$ curves from the modified experimental data of the 400 °C annealed Co/ n -GaAs SBD according to Eq. (12). The first of two GDs curves was drawn using $\sigma_{s0} = 61 \text{ mV}$ and I_0 values in Figure 13 being for the low temperature region in 140–60 K range, and the second curve was drawn using the corresponding I_0 values in Figure 13 and $\sigma_{s0} = 110 \text{ mV}$ for high temperature region in 140–320 K range.

2.3.2. The determination of series resistance value in the MS rectifying contacts

We have stated above that there are a number of methods helping to determine the series resistance R_s of a SBD. One of them is Norde's model [43]. This model evaluates the R_s from the forward branch $I - V$ curves with $n = 1$. Cheung [40] has calculated the R_s value from the room temperature $I - V$ characteristics of the as-deposited W/GaAs diode ($R_s = 18.8 \Omega$ and $n = 1.13$) and 700 °C annealed W/GaAs diode ($R_s = 145.6 \Omega$ and $n = 1.40$). The annealed diode has a highly resistive layer at the W/GaAs interface due to the annealing. Then, we can calculate the R_s value of the $I - V$ curves of the as-deposited Co/ n -GaAs diode in Figure 8 by models of Norde and Cheung, and the R_s value of 400 °C annealed Co/ n -GaAs diode in Figure 10 by only Cheung method [40].

The straight-line part of the forward bias $\ln I$ vs. V plot is confined to the voltage interval $(kT/q \ll V \ll IR_s)$ due to the voltage drop across the R_s of the semiconductor substrate. Then, the linear part of the $\ln I$ vs. V plot may be small due to the voltage drop across the R_s . Therefore, the R_s can arise difficulties in calculation of the ideality factor and SBH from the straight-line part of the $I - V$ plot. If R_s value is large, this linear interval will be too small to obtain a dependable value of the SBH [22,47,76,136,178,195,196]. Therefore, Norde [43] proposed a method to determine value of the series resistance and BH by considering Eq. (1) in section 2.2., and in the situation where the voltage across the diode is greater than $3kT/q$, Norde's function $F(V)$ is

defined as:

$$F(V) = \frac{V}{2} - \frac{kT}{q} \ln \left(\frac{I(V)}{AA^*T^2} \right), \quad (13)$$

where $I(V)$ is current obtained from the I - V curve. The value of the BH of the diode at each temperature can be obtained [43]:

$$\Phi_b = F(V_{\min}) + \frac{V_{\min}}{2} - \frac{kT}{q} \quad (14)$$

and the series resistance is given by

$$R_s = \frac{kT}{qI_{\min}}, \quad (20)$$

where $F(V_{\min})$ is the minimum value of $F(V)$ and the corresponding voltage is $V_{\min}$. Figure 16 shows the $F(V)$ versus V plot plotted using Eq. (13) for the as-deposited Co/ n -GaAs SBD at each temperatures in the case where the TE dominates.

Figure 17 displays the series resistance and BH *vs* temperature curves for the as-deposited Co/ n -GaAs SBD. The BH value at each temperature was calculated using $F(V_{\min})$ and $V_{\min}$ values from the $F(V)$ *vs* V plot was in eqn.(14). The BH *vs* temperature curve by Norde's method for the Co/ n -GaAs SBD will be discussed in the next section in which is the voltage dependent of BH. The R_s value at each temperature was calculated using $I_{\min}$ in Eq. (20). The $I_{\min}$ is value corresponding to $V_{\min}$. As can be seen from Figure 17, the fit equation to the R_s values was obtained as $y = (-0.124x + 226) \Omega$, that is, the R_s value increases with the slope of -0.124 with a reduce in temperature. The R_s value falling on the fit line is 220, 198 and 194 Ω at 80 K, 180 K and 320 K, as can be seen from Figure 17.

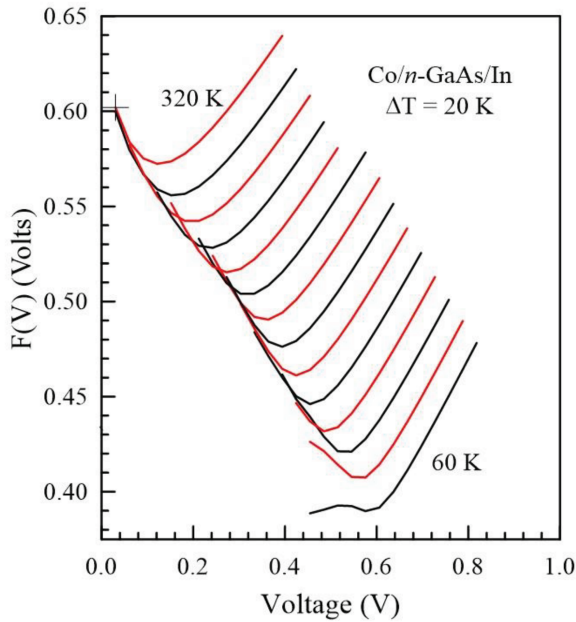


Figure 16. $F(V)$ versus V plot for the as-deposited Co/ n -GaAs SBD at various temperatures for the case where the TE affects.

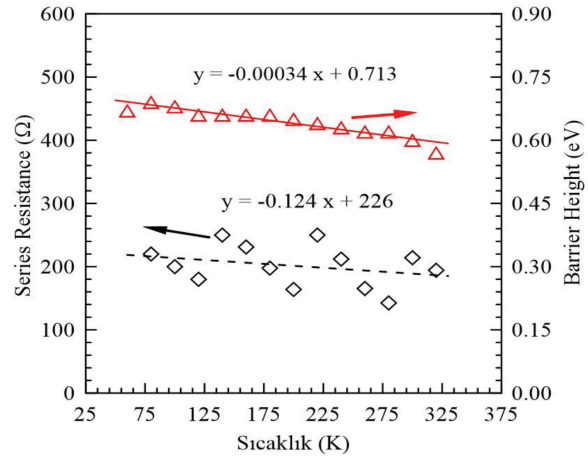


Figure 17. Series resistance and barrier height versus measurement temperature curves for the as-deposited Co/ n -GaAs SBD.

Figure 18 represents the series resistance plots according to Cheung's method [40] for the both Co/*n*-GaAs SBDs. As well-known, the series resistance dominates at high currents rather than low currents at the forward bias $I - V$ curves. The high current region of the forward bias $I - V$ curves is affected from the presence of the R_s . Therefore, there is always a deviation of the ideality depending on the bulk substrate R_s , as would expected. The lower R_s , the greater is a straight line range. Cheung's functions [40] from Eq. (1) are given by

$$V = IR_s + n\Phi_b + n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right), \quad (15)$$

$$\frac{dV}{d(\ln I)} = IR_s + n\frac{kT}{q}, \quad (16)$$

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right), \quad (17)$$

and

$$H(I) = IR_s + n\Phi_B. \quad (18)$$

Eq. (15) is obtained from Eq. (1) in section 2.2. Eq. (16) is the derivative according to $\ln I$ of Eq. (15). The $H(I)$ values in Eq. (18) are calculated of Eqn. (17). We will only determine R_s from $dV/d(\ln I)$ versus I plots.

The values of R_s were obtained from the slopes of the $dV/d(\ln I)$ - I plots drawn in accordance with Eq. (16). As seen from Figure 18, the R_s ranges from 28Ω at 320 K to 59Ω at 60 K for the as-deposited diode, and the R_s ranges from 160Ω at 320 K to 105Ω at 60 K for the annealed diode. It has been seen from tables in Figure 18 that the series resistance of the as-deposited diode is greater than that of the annealed diode at each temperature. The similar examples have also been observed in the unannealed and 700 °C annealed Ni/*p*-InP [193], and unannealed and 700 °C annealed W/*n*-GaAs SBDs [40]. As stated in section 2.3., Cheung [40] have reported the values of $R_s = 18.8\Omega$ and 145.6Ω for the as-deposited and 700 °C annealed W/GaAs diodes, respectively. They [40] attributed the increment in R_s value to highly resistive layer at the W/GaAs interface which forms with the diffusion of W atoms into a depth of about 500 Å of the GaAs substrate after 700 °C annealing. It has been stated also by Tung [60] that many kinetic processes can occur in an MS interface by annealing. Interdiffusion, contamination, chemical reaction, compound formation, interface roughening, defect generation, defect annealing, additive migration, etc. can form at surface layer of the semiconductor substrate or at MS interface during annealing.

Thereby, we can say that a highly resistive layer at Co/GaAs interface forms due to 400 °C annealing. But, the R_s reduces for the 400 °C annealed Co/*n*-GaAs diode while it arises for the as-deposited diode with decreasing measurement temperature. The reduce in the R_s value with a reduce in measurement temperature have also been observed in the Cu/Cu₃Se₂/*n*-GaAs/In [197] and Au/Ti/HfO₂ (10 nm)/*n*-GaAs [33] and Au/Ti/HfO₂ (5 nm)/*n*-GaAs SBDs [198], and furthermore in (Ni/Au)/AlGaIn/GaN/SiC SBDs by Saadaoui et al. [199]. Biyikli et al. [200] have obtained the R_s value increasing with decreasing measurement temperature for the Au/Ti/*n*-GaAs SBD without interfacial layer. Such a discrepancy in temperature dependent R_s value of the Au/Ti/*n*-GaAs SBDs with and without interfacial layer [33,197,198,200] can be ascribed to the chemical interplay of the GaAs substrate with layer onto GaAs as two types of diodes were fabricated from the pieces cut from the same wafer GaAs [15,28,33,34,198]. Some authors [179,197,201] have reported that the resistance

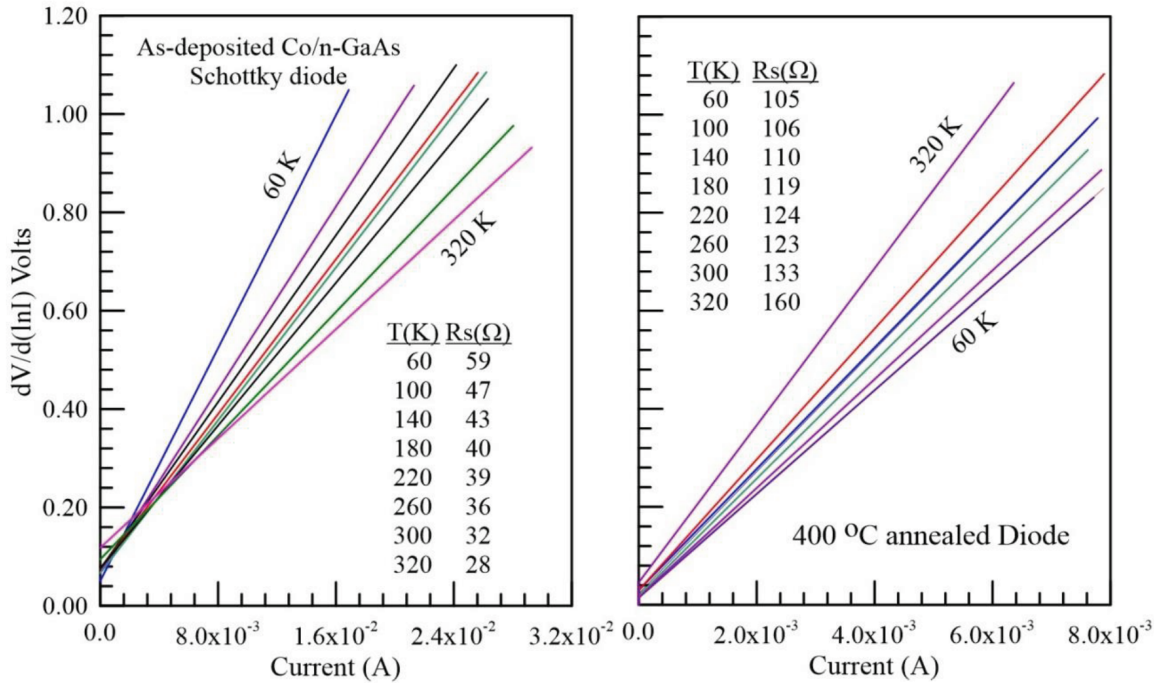


Figure 18. Series resistance plots according to Cheung's method for the both Co/*n*-GaAs SBDs.

of the MS rectifying contact without interfacial layer changes with the free carrier density in the semiconductor substrate, and that the temperature-dependent mobility and energy band gap of the considered semiconductor do not cause to a perceptible potential barrier modification at lower temperatures. Furthermore, they [179,201] have reported by the help of simulated forward bias $I - V$ curves over a wide temperature range that the temperature dependent mobility owing to the lattice scattering gives rise to a reduction in R_s with a reducing in temperature which results in an intersection in the experimental $I - V$ curves at higher currents.

The used method for the most accurate and reliable evaluation of the R_s , ideality factor n and $\hat{O}_b$ is very important because they strongly depend on these methods. The direct calculation from the measured data fails due to the bias dependence of the ideality factor as well as the contribution of excess currents and the series resistance. Norde's and Cheung's method to more accurately evaluate the diode parameters use plots of auxiliary functions. In spite of this, the methods have their own weaknesses as well. Norde's functions assume the n to be very close to unity. This is not generally true for a real SC. To calculate $\hat{O}_b$, it is used only a single point of the graphic of Norde's function. These are the main deficit of Norde's functions [43]. These problems often lead to the overestimation of the series resistance value when compared with the values determined by Cheung's method [40], as the seen from the R_s values we have obtained by both methods above. It can be said that the $\hat{O}_b$ is bias voltage-dependent BH because it is calculated from Eq. (14) which consists of $F(V_{min})$ and V_{min} , not from the saturation current I_0 corresponding to $V = 0$. It can be seen from Figure 17 that the $\hat{O}_b$ arises with reduce of temperature. Cheung's method requires good linearity of $dV/d(\ln I)$ versus I curve for accurate extraction of parameters, but this one seems to be the most reliable and accurate among the discussed methods. Furthermore, Cheung and Cheung [40] used supported their analysis in addition with the function given in Eq. (18) [41,47,49,50,128,202–206]. Oruç and Altındal [50] have compared the methods used for determination of the R_s with each other, considering the $I - V$ characteristics of Au/FePc/*p*-Si SBD, and have reported that

the accurate determination of the SBD parameters strongly is very related to the used method. Although the Norde's method leads to some improvements, its accuracy depends on selected α value. However, it has been noted that the Cheung method displays some advantages because it has a very simple use.

2.3.3. The bias dependent-barrier height in the lateral inhomogeneity models

2.3.3.1. The lateral inhomogeneity model suggested by Tung and coworkers

The forward current of a real SBD has been reported to arise from two current components under the pinch-off model in the literature [20,63–65]. One of them is current with a lateral homogeneous BH across the entire contact area. The second component is current related to some small local region (patches) with low BH. In low sample temperature and bias voltage measurement case, this second current component has much greater R_s than the first one because of the local pinch-off effect around the available patches, so it usually prevails only in the small current region. Therefore, the low SBH-patch parameters can be obtained from the temperature dependent $I - V$ data and it can be said that the SBH homogeneity may be related to the interface properties [60,65,86,98,107,108,113,207–209].

The SB homogeneity has attracted increasing attention both scientifically and technologically. It has been successfully applied the model proposed by Tung [20,63–65] in the inspection of the temperature dependent measurements of the SCs. Even so, some arguments related to the pinch-off model in electron transport event have emerged. The SBH change at the MS interface indicates the change of the potential from region to region. It has been seen from the explanations above that the suggestions related to Schottky barrier inhomogeneity are much important in the explication of the real $I - V - T$ curves and in explanation of the appeared deviations from the commonly known conventional TE theory. Tung [20,65] has considered a system of “patches” with the low barrier height embedded in a higher uniform barrier area. The size of the patches is accepted to be small compared to the size of the depletion region for a pinch-off effect to arise [65,107,108].

Figure 19 shows the energy-band diagram of a Schottky rectifying contact at zero bias condition; where eV_n is the energy difference between Fermi energy Level (E_f) and the CB energy minimum of semiconductor in the neutral region, $e\Phi_{b0} = e(V_b + V_n)$ is the zero bias SBH or lateral homogeneous barrier height and it is defined as the energy different between the CB minimum and Fermi Level E_{fm} at the metal side; V_b is diffusion potential the value at the zero-bias. $\Delta\Phi$ is the difference of the uniform BH Φ_{hom} with the low BH [93,207]. Tung and coworkers [20,60,64,65,107,108] have tread the numerical simulations and have extracted a set of analytic equations to define the temperature-dependent $I - V$ nature of pinched-off effect.

The diffusion potential distribution along the z -axis for circular patches with the radius R_0 at MS interface can be taken as [60,65]:

$$V(0, z) = V_b \left(1 - \frac{z}{W}\right)^2 + V_n + V - \Delta\Phi \left[1 - \frac{z}{(z^2 + R_0^2)^{1/2}}\right], \quad (19)$$

where $V_b = (\Phi_{hom} - V_n - V)$ is the band bending due to the MS contact with a uniform BH Φ_{hom} , V_n is the potential difference between Fermi Level and the CB minimum of semiconductor in the neutral region, V is the applied voltage, W is the depletion width defined as $(2\varepsilon_0\varepsilon_s V_b / qN_d)^{1/2}$ where ε_s is the dielectric constants of the bulk material.

The experimental results have shown the modification of barrier height (BH) with the bias [15,34,60,92,207]. In Figure 20, the diffusion potential changes from the reverse bias of -0.20 V to forward bias of 0.20 V at 0.10 V

intervals. Note that the saddle point potential or $e\Phi_{b,patch}$ (Figure 19) rises with forward branch bias and thus the current decreases with increase of the bias; and $e\Phi_{b,patch}$ reduces with reverse branch and thus the current arises and unsaturates with increase of the bias. The bias dependent $I - V$ curves in Figure 20 are plotted using Eq. (19). However, the basis of pinch-off model plays an important role in carrier transport. The dependence of the potential on applied bias voltage may be a key enabling us to understand the reasons of the observed abnormalities in $I - V$ measurements [60,65]. It has been concluded from the experimental on the $I - V$ data that there is a larger saddle point potential change in the forward bias case than that in reverse bias case, at the same amount of the bias voltage [99]. That is, at forward (reverse) applied bias, the rise (decrease) in the saddle point potential leads to an increase (decrease) in the effective BH that decreases (increases) the current transport with the applied voltage.

Ru et al. [99] have studied the NiSi/*n*-Si SCs with different barrier inhomogeneities to investigate the bias dependence of the BH. Their experimental data have shown that the effective BH severely depends on the barrier inhomogeneity and the bias voltage. The decrease of effective BH arises as the bias changes from forward to reverse branch, implying that the current transport has severely been affected from the pinch-off or the existence of saddle point in the Schottky barrier region [99]. Therefore, Ru et al. [99] have reported that the pinch-off effect under forward bias is stronger than that under reverse bias. Thus, it has been concluded that the effective BH under forward bias should be higher than that under reverse bias when considering Tung's model [20,60,65]. They have mentioned that this effect technologically seems to do no good for the Schottky diode as a rectifying device because a Schottky diode ideally requires a low-barrier diode for forward branch and a high-barrier diode for reverse branch. According to this model, a Schottky diode with inhomogeneous barrier height may behave like a high-barrier rectifier at forward branch and a low-barrier rectifier at reverse branch [93,94,99,103,112,113,207].

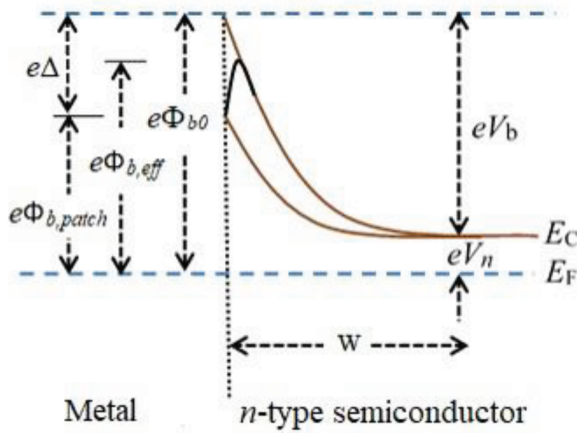


Figure 19. The effective barrier height at a pinched-off $e\Phi_{b,eff}$ is slightly smaller than that behind a spatially homogeneous high barrier-height region, $e\Phi_{hom} = e\Phi_{b0}$, but is much larger than the barrier height behind a spatially low barrier-height region, $e\Phi_{b,patch}$.

For small and circular patches, Tung [60,65] has assumed a GD of low-SBH circular patches described by a distribution of γ with standard deviation σ_T , Tung [60,65] have given the total forward bias current as:

$$I = AA^*T^2 \exp(-\beta\Phi_{bo}^{hom}) [\exp(\beta(V - IR_s)) - 1] [1 + P(I)] , \quad (20)$$

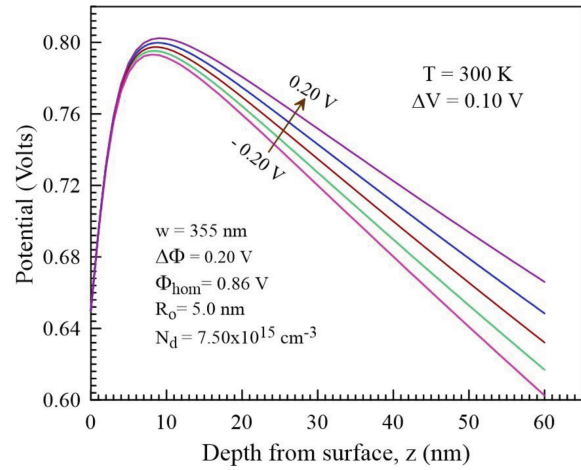


Figure 20. Variation curves of the diffusion potential for the bias dependent patches from metal contact to the inside of the semiconductor bulk material in a MS Schottky contact.

where $V \leq 3kT/q$. The other terms than $[1 + P(I)]$ on the right side of Eq. (20) are the TE current of a homogeneous SC with area A , the homogeneous BH Φ_{bo}^{hom} ; moreover $\beta = q/kT$. The $P(I)$ in Eq. (20) is a function related to the patch density ρ and patch strength factors γ . The quantity γ is stated as

$$\gamma = 3 (R_p^2 \Delta_p / 4)^{1/3}, \quad (21)$$

where Δ_p is the barrier reduce at the saddle point in front of a circular patch with radius R_p at the interface. The strength parameter γ has a GD for $\gamma \geq 0$, the term $P(I)$ in Eq. (20) can be given as [60,65]

$$P(I) = \frac{8\pi\rho\sigma_T^2\eta^{1/3}}{9(V_b - V + IR_s)^{1/3}} \exp\left(\frac{\beta^2\sigma_T^2(V_b - V + IR_s)^{2/3}}{2\eta^{2/3}}\right), \quad (22)$$

where σ_T is the standard deviation of γ around zero and $\eta = \varepsilon_s \varepsilon_o / qN_d$, ε_s and N_d are the dielectric constant and the free carrier density of the semiconductor substrate, respectively. V_b is the interface band bending of the homogeneous barrier outside the patch, and ρ is the circular patch density. Thus, Eq. (20) defines the modulated TE current through inhomogeneous SCs with circular patches. Consequently, the expression in Eq. (20) gives the current over the SC with a homogeneous Φ_{bo}^{hom} and an A area, and plus the current of the low-BH patches.

The an effective SBH in [60,65]

$$\Phi_{eff} = \Phi_{bo}^{\text{hom}} - \Delta\Phi, \Delta\Phi = \frac{\sigma_T^2}{2kT} \left(\frac{V_{bo}}{\eta}\right)^{2/3}. \quad (23)$$

The n for a current defined by Eq. (23) is expressed as

$$n \approx 1 + \Delta n, \Delta n \approx \frac{\sigma_T^2 V_{bo}^{-1/3}}{3kT\eta^{2/3}} \quad (24)$$

and the effective area A_{eff} of the low barrier height-patch is given by

$$A_{eff} = \frac{8\pi\sigma_T^2}{9} \left(\frac{\eta}{V_b}\right)^{1/3}. \quad (25)$$

The pinch-off occurs when the condition is satisfied by [65]

$$R_p < \frac{W\Delta\Phi}{2V_b}. \quad (26)$$

Figure 21 represents the diffusion potential change for patches with different BH difference. When the $\Delta\Phi$ is lower than the critical value, the pinch-off effect does not occur. A critical radius for pinch-off can be stated with Eq. (26). The pinch-off effect increases as $\Delta\Phi$ increases. When $\Delta\Phi$ is close zero, the potential shape is same as that of a Schottky contact with lateral homogeneous barrier height.

Figure 22 represents the diffusion potential change for patches with radius R_p . As seen from Figure 22 and Eq. (26), the patches become more pinched-off with reducing low-BH patch radius, and thus the saddle

point potential increases. When the patches are much larger than the critical size, the potential distribution approaches that of a lateral homogeneous MS contact with the same BH as that of the low-BH patch. Thus, the smaller the radius of the low barrier patch, the easier it is to obtain pinch-off conditions. Therefore, the current across the Schottky contact is affected by the low barrier regions even in the pinch-off regime [65,97,209].

We have investigated the influence of the patch density on the current transport, and have plotted the forward and reverse bias $I - V$ curves for a metal/ n -GaAs rectifying contact by help of Eq. (20) in Figure 23. The patch density ρ has been varied from $1.12 \times 10^9 \text{ cm}^{-2}$ to $1.12 \times 10^{12} \text{ cm}^{-2}$ for the same standard deviation of $\sigma_T = 2.56 \times 10^{-5} \text{ cm}^{2/3} \text{ V}^{1/3}$. But, the σ_T for the patch parameter may change from diode to diode. The reverse and forward bias current at a given voltage arise, and n value arises and BH value decreases with arising patch density. The nonsaturating behavior of curves in the reverse bias reduces with decrease in the patch density because the slope of the linear part of the curve with the patch density value of $\rho = 1.12 \times 10^9 \text{ cm}^{-2}$ is 2.25 while that of the curve with $\rho = 1.12 \times 10^{12} \text{ cm}^{-2}$ is 2.40.

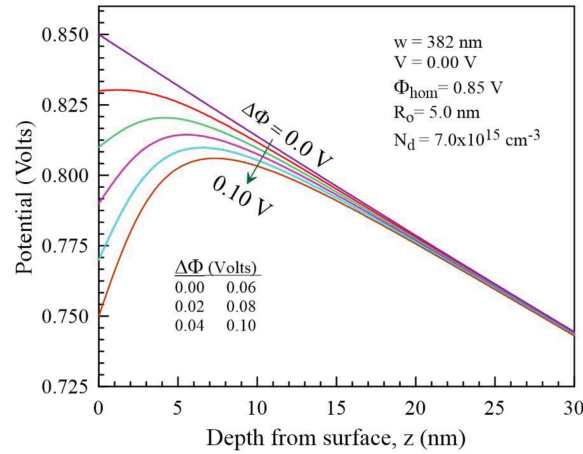


Figure 21. Change of the diffusion potential for patches with different barrier height difference from the MS interface to the inside of the semiconductor.

2.3.3.2. The lateral inhomogeneity model suggested by Werner-Güttler and Song

As stated in detail above, the SB inhomogeneity has attracted increasing attention from both scientific and technological points of view. Assuming barrier height with a GD is one of the successful models which explains a lot of abnormal behaviors of the $I - V$ and $C - V$ characteristics of the real SBDs. The made theoretical analyzes on models of Werner-Güttler model [57] and Song [105] have shown that the mean BH reduces with increasing bias and decrease temperature in the forward branch. This contradicts with the existing models and experiments related to the electrical behavior of SCs. Whereas, most of the anomalous behaviors in current transport of the SBDs have been explained by this model. If we want to say more precisely, when the temperature-dependent current curves have been plotted by help of Werner-Güttler model, it has been observed that the current at lower temperatures may exceed the current at higher temperatures and high voltage [210–213]. Osvald [213] has reported that the intersection point of $I - V$ curves at different temperatures is not caused by higher ideality factors of the curves; the ideality factor of inhomogeneous diodes remains unity when the constituting single diodes also have an ideality factor of unity. This intersection is caused by the temperature dependence of the apparent BH itself. Then, in the forward $I - V$ curves of noninteractive inhomogeneous SDs, it has been showed [167,168] that this problem can be solved by considering the bias dependence of apparent

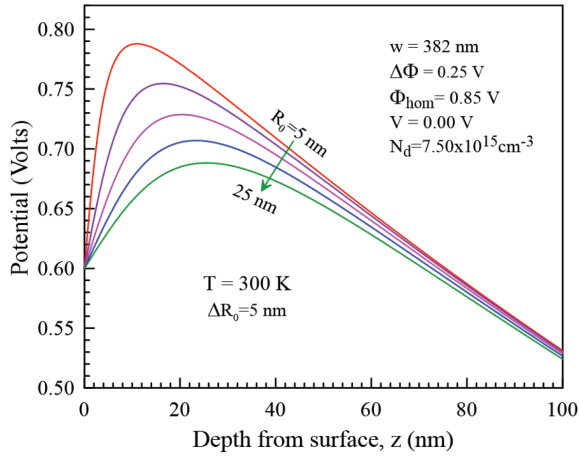


Figure 22. Change of the diffusion potential for patches with patch radius R_p from the MS interface to the inside of the semiconductor.

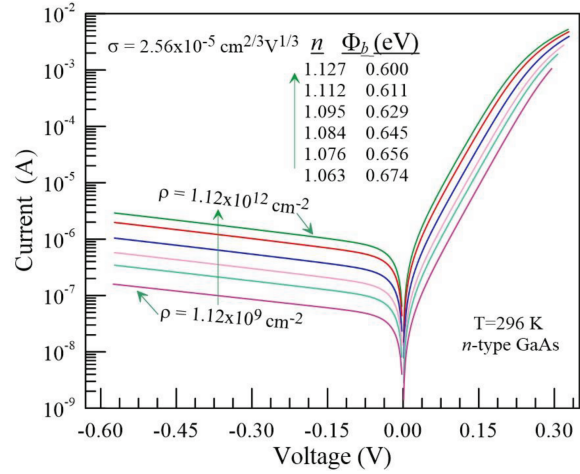


Figure 23. The reverse and forward branch $I - V$ curves by help of Eq. (20), of an inhomogeneous n - type GaAs SBD with $\Phi_{bo}^{hom} = 0.72$ eV, $R_s = 12 \Omega$, $\sigma_T = 2.56 \times 10^{-5} \text{ cm}^2/3 \text{ V}^{1/3}$, $N_d = 2.51 \times 10^{17} \text{ cm}^{-3}$, $A = 0.0141 \text{ cm}^2$ and $V_{bo} = 0.67$ eV and $T = 296$ K. The ρ has been ranged from $1.12 \times 10^9 \text{ cm}^{-2}$ to $1.12 \times 10^{12} \text{ cm}^{-2}$. These values are 1.12×10^9 , 5.12×10^{10} , 1.12×10^{11} , 3.12×10^{11} , 7.12×10^{11} , $1.12 \times 10^{12} \text{ cm}^{-2}$.

BH in Werner-Güttler's model which consists of the ideality factor quantity [57]. Some authors [213–215] have suggested the different solutions to overcome this problem.

Let us reconsider the forward bias TE current expression for a SBD. We can write this expression as follows

$$I = AA^*T^2 \exp\left(-\frac{q\Phi_b(0,T)}{kT}\right) \left[\exp\left(\frac{qV_D}{nkT}\right) - 1\right], \quad (27)$$

where $V_D = (V - IR_s)$, V is the forward-bias voltage, IR_s and V_D are the voltage drop across the R_s and the depletion region, respectively, $\Phi_b(0,T)$ is the zero bias BH at a given temperature. When the BH is bias-dependent, $\Phi_b(0,T)$ in Eq. (27) should be written as $\Phi_b(V,T)$ at a given temperature. The forward bias BH arises with increment of the bias voltage. We suppose that the BH distribution at inhomogeneous SCs is defined by the GD. Now, the ideality factor n is stated as [87,123,127,137,216]

$$(n^{-1}(T) - 1) V_D = -\Delta\Phi_b(V,T), \quad (28)$$

where $\Delta\Phi_b(V,T)$ is the change of the BH under bias, and it is written as [123,167,168]

$$\Delta\Phi_b(V,T) = \Phi_b(V,T) - \Phi_b(0,T). \quad (29)$$

Eq. (29) represents that bias-independent n involves the fact that $\Phi_b(V,T)$ linearly arises with the bias. Therefore, the barrier change is given as

$$\Delta\Phi_b(V,T) = \rho_1(T)V_D \quad (30)$$

$$n^{-1}(T) - 1 = -\rho_1(T) \quad (31)$$

here $\rho_1 > 0$ and it is a voltage coefficient. The BHs in Eq. (29) can be written as [123,167,168]

$$\Phi_b(0, T) = \bar{\Phi}_b(0, T) - \frac{q\sigma^2(0)}{2kT} \quad (32)$$

$$\Phi_b(V, T) = \bar{\Phi}_b(V, T) - \frac{q\sigma^2(V)}{2kT}, \quad (33)$$

where $\bar{\Phi}_b(0, T)$ and $\bar{\Phi}_b(V, T)$ are mean BH values of the GD at a given temperature. Now, using Eqs. (29), (32) and (33), the variation of the bias dependent BH can be stated by

$$\begin{aligned} \Delta\Phi_b(V, T) &= \Phi_b(V, T) - \Phi_b(0, T) \\ &= \bar{\Phi}_b(V, T) - \bar{\Phi}_b(0, T) - \frac{q(\sigma^2(V) - \sigma^2(0))}{2kT} \\ &= \Delta\bar{\Phi}_b(V, T) - \frac{q\Delta\sigma^2(V)}{2kT} \end{aligned} \quad (34)$$

Thus, using Eqs. (28) and (34), the ideality factor for single-GD is found as

$$(n^{-1}(T) - 1) V_D = -\Delta\bar{\Phi}_b(V, T) + \frac{q\Delta\sigma^2(V)}{2kT} \quad (35)$$

or

$$(n^{-1}(T) - 1) = -\rho_2 + \frac{q\rho_3}{2kT}, \quad (36)$$

where [70,123,137]

$$\Delta\bar{\Phi}_b(V, T) = \bar{\Phi}_b(V, T) - \bar{\Phi}_b(0, T) = \rho_2 V_D, \quad (37)$$

$$\Delta\sigma^2(V) = \sigma^2(V) - \sigma^2(0) = \rho_3 V_D. \quad (38)$$

If the mean BH $\bar{\Phi}_b$ as well as the σ^2 varies linearly with the bias, then, the ideality factors can be independent of bias. The quantities ρ_2 and ρ_3 are the voltage coefficients of the mean BH and the standard deviation, respectively. The forward bias $I - V - T$ data obey the GD of BHs, the $(n^{-1}-1)$ vs. $(2kT)^{-1}$ gives a straight line with the slope and y -axis intercept of the voltage coefficients ρ_2 and ρ_3 , respectively, as can be seen from Eq. (36). The value of ρ_3 mentions that the BH distribution becomes more homogeneous with increasing voltage. Consequently, substituting $\bar{\Phi}_b(VT)$ and $\sigma^2(V)$ from Eqs. (37) and (38) in Eq. (33), the bias-dependent $\Phi_b(V, T)$ for the single-GD at any temperature is found as [88,137,167,168]

$$\Phi_b(VT) = \bar{\Phi}_b(T) - \frac{q\sigma^2(0)}{2kT} + \left(\rho_2 - \frac{q\rho_3}{2kT}\right) V_D. \quad (39)$$

If the $\Phi_b(V, T)$ instead of $\Phi_b(0, T)$ in Eq. (27) is written, then Eq. (27) can be arranged as

$$I = AA^* T^2 \exp\left(-\frac{q\Phi_b(V, T)}{kT}\right) \left[\exp\left(\frac{qV_D}{kT}\right) - 1\right], \quad (40)$$

Chand [199,205] has used Eqn. (27) (for $n = 1$) and Eq. (32) to draw the low temperature $I - V$ data of SCs and has reported an unexpected observation. It can be seen from Figure 24 that the current at low temperatures has exceeded the current at high temperatures from the obtained $I - V - T$ curves [210–213]. The

same result has also been confirmed by the some authors [167,168,215]. Chand [199,205] has reported that no such a crossing arises in the curves with higher ideality factor n at low temperatures and has stated that the high n results in by the bias dependence of the SBHs. It is well-known that the bias dependence of SBHs causes the temperature-dependent n in the inhomogeneous SCs. Thereby, it has been reported in Refs. [167] and [168] that, if Eqs. (39) and (40) are used, no such a crossing arises in the $I - V$ curves at low temperatures. This case can be seen in Figure 25.

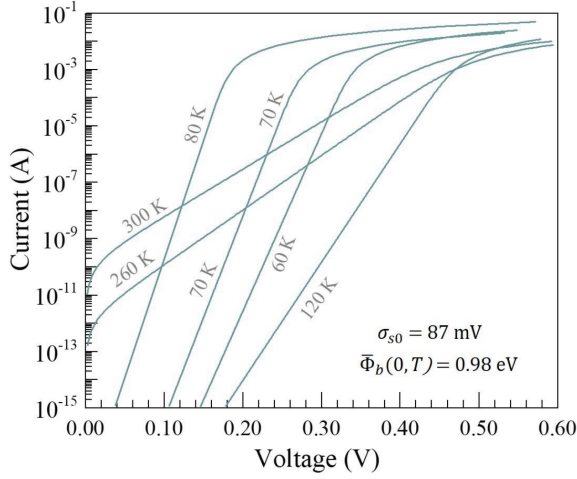


Figure 24. Calculated forward bias $I - V$ curves of a SC using Eqs. (27) and (32) for various temperatures.

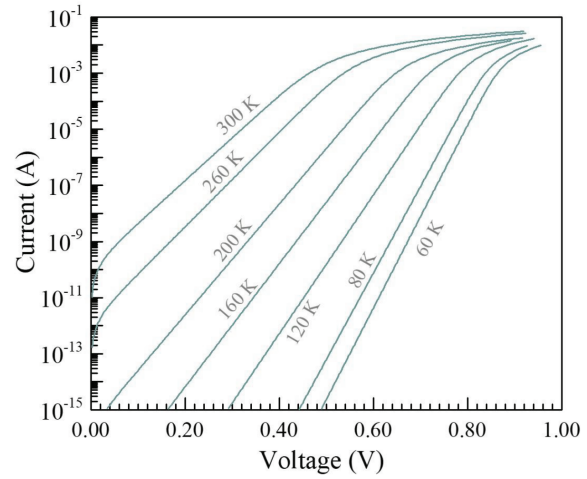


Figure 25. Calculated forward bias $I - V$ characteristics of a SC using Eqs. (39) and (40).

Figure 24 represents the calculated forward bias $I - V$ curves of a SC using Eqs. (27) and (32) for some temperatures. Eqs. (27) and (32) give the total current through a SC with the inhomogeneous BH for $n = 1$ which has the GD of BHs. The calculated $I - V$ curves thus using $\bar{\Phi}_b(T) = 0.98$ eV and $\sigma_{s0} = 87$ mV values for various temperatures are shown in Figure 24, $A^* = 8.16$ Acm⁻²K⁻² of n -GaAs, $A = 0.0177$ cm². Figure 25 displays the calculated forward bias $I - V$ curves of a n -type GaAs SC. These plots have been drawn using Eq. (40) for some temperatures with $\bar{\Phi}_{bo} = 0.82$ eV and $\sigma_{so} = 66$ mV and $\rho_2 = -0.21$, $\rho_3 = -0.0042$ V in 60–120 K range, and with $\bar{\Phi}_{bo} = 0.98$ eV and $\sigma_{so} = 87$ mV and $\rho_2 = 0.157$, $\rho_3 = -0.0126$ V in temperature range of 120–300 K, due to the presence of two GDs in low and high temperature regions. Thus, it has been observed that the discrepancies reported by some authors [167,168,215] can be removed by regarding the bias dependence of the BH according to the GD model of the inhomogeneous barriers. In section 2.2, the experimental and theoretical bias dependent semilog reverse $I - V$ curves have been drawn by using conventional TE equation and following the same idea.

3. The capacitance-voltage characteristics in Schottky barrier diodes

In the $C - V$ measurements, a small constant sinusoidal voltage is also superimposed on the dc junction voltage when a forward or reverse bias dc voltage is applied on the junction. As known, the ideal $C - V$ data of a SBD is independent of the frequency of the small constant sinusoidal voltage and it arises with increment of the forward voltage. This ideal case is often disrupted due to the R_s and the existence of the interface states and native oxide layer between the MS interface [29,36–38], and [11,39–41].

The bias dependent-surface potential Ψ_s at the semiconductor side in MIS contacts by following Refs. [8,11,127,219] can be written as

$$\Psi(V) = \Phi_B - c_2 V + IR_s - V_p, \quad (41)$$

where ideality factor $n = 1/c_2$. The space charge density in Schottky depletion layer is given by

$$Q_{sc}(V) = -[2q\varepsilon_s N_A \Psi_s]^{1/2}, \quad (42)$$

where N_A is the free carrier density of the p -type semiconductor, ε_s the permittivity of the semiconductor. At very high frequency (HF) capacitance-voltage ($C - V$) data, there is no contribution of the interface state charge to diode capacitance C because they cannot follow an a.c. signal and they are in interaction with the semiconductor [11,127,220–222]. The exact circuit of diode will be the oxide layer and depletion capacitance in series. This will occur when the time constant is too long to allow the charge to move in and out of the interface states in response to a signal. The C of the MIS diode per area unit is represented by

$$C = \frac{dQ_{sc}}{d\Psi_s} \frac{d\Psi_s}{dV}. \quad (43)$$

Using Eqs. (41)–(43) without taking into account the R_s effect, the C is given by

$$C = c_2 \left[\frac{q\varepsilon_s N_A}{2(\Phi_B - c_2 V - V_p)} \right]^{1/2} \quad (44)$$

or

$$\frac{1}{C^2} = \frac{2(\Phi_B - c_2 V - V_p)}{qc_2^2 \varepsilon_s N_A}. \quad (45)$$

According to this equation, the capacitance plot is a straight line, the intercept with the voltage axis is V_o and the slope also is c_2 . Thus barrier height and c_2 , respectively, are represented by:

$$\Phi_B^{cv} = c_2 V_o + V_p, \quad (46)$$

$$c_2 = \frac{2}{q\varepsilon_s N_A [d(C^{-2})/dV]}. \quad (47)$$

The value of c_2 for an ideal SBD without the interfacial layer is equal to one. Thus Eqs. (44) and (46) are given by

$$C = \left[\frac{q\varepsilon_s N_A}{2(\Phi_B - V - V_p)} \right]^{1/2} \quad (48)$$

$$\Phi_B^{cv} = V_o + V_p, \quad (49)$$

Figure 26 displays the capacitance plots of one of the MS and MIS Pb/ p -Si/Al SDs for 1.0 MHz and 296 K which are given in Figure 3. The MIS contact in Figure 26 is always larger (in magnitude) than the MS contact slope giving a higher doping level than is actually present [136,220,223,224]. That is, the slope of the MS is lowered than slope of the MIS contact by a factor of c_2 , or by the relation of the theoretical carrier density $N_{A, MIS}$ and $N_{A, MS}$ doping density known as [11,223]

$$c_2 = \frac{N_{A, MIS}}{N_{A, MS}} \quad [50]$$

In this case, the population of the interface state density is governed entirely by the semiconductor but the interface states cannot follow an ac signal because the $C - V$ measurements have been made at very high frequency. The values of $N_{A, MIS} = 3.98 \times 10^{15} \text{ cm}^{-3}$ and $N_{A, MS} = 4.78 \times 10^{15} \text{ cm}^{-3}$ were obtained from the slopes of the C^{-2} vs. V curves of the MIS and MS diodes in Figure 26, respectively. Thus, the value of 0.829 for c_2 is found considering Eq. (50), that is, a value of $1/c_2 = n = 1.206$ for the MIS diode. This $1/c_2 = n$ value is a value close to $n = 1.19$ obtained from the forward bias $I - V$ curve of the same MIS diode in Figure 3 in section 2.2.

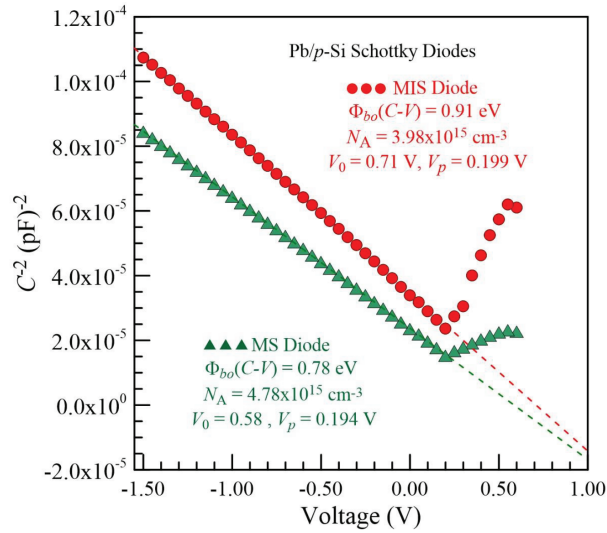


Figure 26. Capacitance versus voltage curve of one of the MS and MIS Pb/*p*-Si/Al SDs for 1.0 MHz and 296 K, the $I - V$ characteristics of which are given in Figure 3 in section 2.2.

The value of 0.829 for c_2 and the intercept values of $V_o = 0.58$ and $V_o = 0.71$ Volts and $\Phi_B^{cv} = 0.78$ eV and $\Phi_B^{cv} = 0.91$ eV for the MIS and MS diodes are the values obtained from the C^{-2} vs. V curves in Figure 26, respectively. Thus, a value of $\Phi_B^{cv} = 0.79$ eV for the MIS diode was found considering c_2 is in Eq. (46). That is, Φ_B^{cv} value for a Pb/*p*-Si MS diode without the interfacial layer should be 0.79 eV which is a value close to $\Phi_B^{cv} = 0.78$ eV obtained for the MS diode $\Phi_B^{cv} = 0.78$ eV. Moreover, the values of 0.71 and 0.72 eV for the MS and MIS Pb/*p*-Si diodes are found from the $I - V$ curves in Figure 3, respectively. The $\Phi_B^{cv} = 0.78$ eV is higher than the value of $\Phi_B^{IV} = 0.71$ eV, as expected. The capacitance is insensitive to potential changes on a lesser length scale than the space-charge width and the capacitance measurements take an average over the total Schottky contact area. The current across the contact changes exponentially on the potential barrier and thus depends sensitively on the detailed barrier distribution across MS Schottky contact. Any change in the lateral barrier height requires the current to flow preferably through the barrier minima. Consequently, the spatial fluctuations of band bending V_p and Φ_{bp} give different SBH for the both methods [123,225]. That is, the $C - V$ measurement gives an average value of lateral high and low barrier heights across the diode. Tung [226] has stated that the difference between Φ_B^{cv} and Φ_B^{IV} values is also evidence for the barrier inhomogeneity. Bati et al. [227] have experimentally given the information about the forward biased excess capacitance in SBDs. They have determined experimentally that the excess capacitance in the forward bias $C - f$ curves of MIS and

intimate Schottky contacts with perfect or imperfect ohmic back-contact, respectively, the excess capacitance arises by interface or minority carrier or both [228].

The series resistance R_s also plays an important role in the behavior of their experimental $C - V$ of the SBDs [38,42,229–231]. The presence of a peak in the forward $C - V$ curves have been reported in some investigations. Chattopadhyay et al. [11,42] have ascribed the origin of such a peak to the interface states density (N_{ss}) and the R_s effect. Later, some authors [229,230] have obtained the similar equations to those given by Chattopadhyay for the admittance properties of the SBDs. Karataş and Türüt [231] have realized the analysis of capacitance and conductance–frequency (C - G -frequency) characteristics Zn/ p -Si Schottky diodes by admittance spectroscopy following Refs. [42,229,230]. They have reported the effect of the series resistance in determining the ISDD and especially their relaxation time in the SDs with high resistivity, and have mentioned the importance of the R_s on the C - G -frequency characteristics of the experimental and theoretical data. As mentioned above, Chattopadhyay and Raychaudhuri [42] have, in detail, investigated the capacitance peak value in the forward bias $C - V$ characteristics of SBDs to vary with the R_s , N_{ss} and frequency; and that the effect of R_s on the C is found appreciable at HF. On the other hand, in the C - G -frequency curves with the R_s as a parameter, the G of the diode arises and C reduces with frequency due to the series resistance effect in the high frequency limit. This variation in the G limits the use of well-known the G method to obtain N_{ss} without considering the series resistance effect [38,42,229–231].

3.1. The temperature dependence of capacitance-voltage characteristics

Figure 27 demonstrates the temperature dependent $C^{-2} - V$ curves of the MS Pb/ p -Si/Al SD at 1.0 MHz. Figure 28 displays the temperature dependent $C^{-2} - V$ curves of the MS Pb/ p -Si/Al SD at 1.0 MHz. The value of Φ_B^{cv} arises with decreasing temperature. It is seen that the Φ_B^{IV} from the $I - V$ curves is lower than the average of the SBH from the capacitance curves. Furthermore, this is more pronounced at lower temperatures, as can be seen from Figure 28. Since Φ_B^{cv} is the mean barrier height which approximately equals to the lateral homogeneous barrier height, as can be seen in [123,225], the measured SBH for SB diode will be related to the measurement method. The presence of one or several of some effects which cause nonideality of the diode parameters can make difficult an accurate determination of the Φ_B^{cv} SBH [21,73,200,225,232].

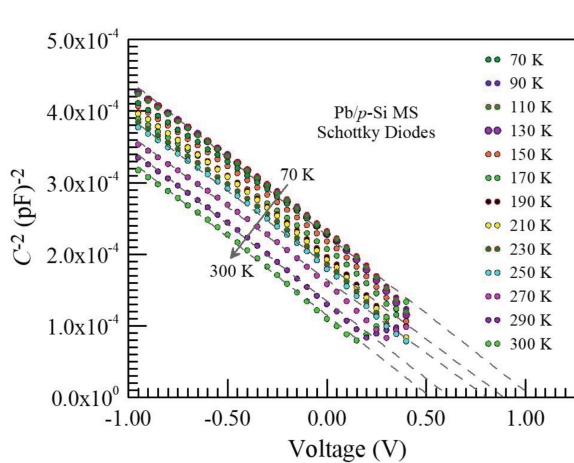


Figure 27. Temperature dependent $C^{-2} - V$ curves of the MS Pb/ p -Si/Al SBD at 1.0 MHz.

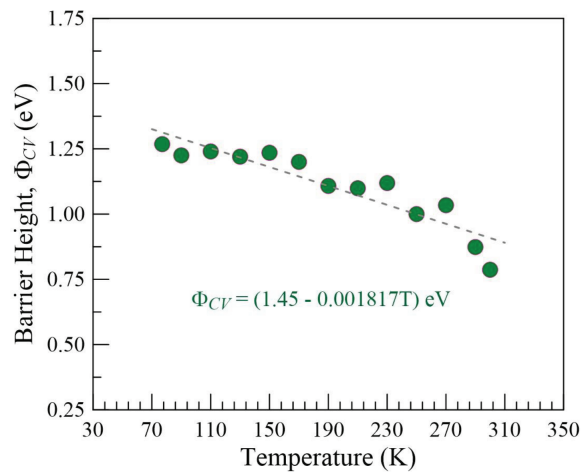


Figure 28. Temperature dependent $C^{-2} - V$ curves of the MS Pb/ p -Si/Al SD at 1.0 MHz.

Osvald et al. [214] have simulated the forward and reverse biases $C - V$ dependence of inhomogeneous SBDs. They have concluded the results that inhomogeneous SBDs which have the mean BH equal to the BHs of equivalent homogeneous diodes have very similar $C - V$ characteristics and differ merely remarkably only at forward bias, and that the $C - V$ characteristics of both diodes have an exceptional capacitance peak at forward bias, but not at reverse bias; and that the sign of negative capacitance has been not observed, which are appeared by other reasons than a mobile charge carrier redistribution in the semiconductor space charge region. Duman et al. [235] have measured $C - V - T$ characteristics of the Ni/ n -type 6H-SiC SBDs in 120–500 K range and determined a BH value of 1.36 eV for this diode from $C - V$ measurement at 300 K and 50 kHz. They have reported that the Φ_B^{cv} from the $C - V$ curves does not exhibit temperature dependence in 260–500 K range, while it changes slightly with decreasing temperature between 120 and 260 K. Aboelfotoh et al. [236] have determined the SBH of Ti, Ni, Cu, and Au on n - and p -type Si-terminated 6H-SiC in 150–500 K range, and obtained that the SBH to n -type 6H-SiC does not change with the change of the temperature, while the variation in the SBH with temperature for p -type 6H-SiC monitors very closely the change in the indirect energy gap in 6H-SiC, and have mentioned that chemical bonding at the MS interface is decisive in the SBH variation. They have stated that their findings are incoherent with the SB modification models determined by the charge neutrality level; and moreover, that their findings cannot be accommodated with a defect pinning mechanism, opposite to previous results on III-V semiconductors.

4. Conclusion

A literature summary on the $I - V$ and $C - V$ characteristics of the SBDs and the reasons of their nonideal behaviors has been given in “Introduction” section. It has been emphasized how the characteristics diode parameters are obtained from the $I - V$ and $C - V$ characteristics using the required equations. The reasons of the fact that the calculated values of these diode parameters have extracted different from the expected ones have been interpreted by a GD function of the spatial variation of SBHs presented by Song [105] and Werner and Guttler [57]; and by means of the pinch-off model of Tung and coworkers which arises by interaction of the neighbor “patches” with low barrier placed in a higher uniform barrier area [64,65,108]. It has been accentuated that these models can be successfully applied in analysis of electrical characteristics of various Schottky diodes using the modified TE current theory.

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